INVESTIGATION OF SCHOTTKY BARRIER/MOS SOLAR CELLS ON P—TYPE SILICON WITH Al, Cr, Sn METAL CONTACTS.

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By
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AUGUST, 1977

CERTIFICATE

This is to certify that the thesis entitled, "INVESTIGATION OF SCHOTTKY BARRIER/MOS SOLAR CELLS ON P-TYPE SILICON WITH Al, Cr, Sn METAL CONTACTS" by Satya Priy Joshi is a record of work carried out under my guidance and has not been submitted elsewhere for a degree.

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LIST OF SYMBOLS

A^{**}	Effective Richardson's constant, $A/cm^2/°K^2$
AM1	Air mass one solar radiation, mW/cm^2
C	Capacitance, F
E_c	Conduction band edge, eV
E_g	Semiconductor band gap, eV
E_{FM}	Metal Fermi level, eV
E_{FS}	Semiconductor Fermi level, eV
E_V	Valence band edge, eV
G	Conductance, mho
h	Planck's constant, eV. sec
I_D	Diode current, A
I_L	Light generated current, A
I_{sc}	Short circuit current, A
J_D	Diode current density, A/cm^2
J_L	Light generated current density, A/cm^2
J_{sc}	Short circuit current density, A/cm^2
K	Boltzmann's constant, eV/°K
N_A	Acceptor impurity concentration, cm^{-3}
n	Diode ideality factor
P_{max}	Maximum power obtainable from the cell, W/cm^2
P_{in}	Input power, W/cm^2

q	Electronic charge, C
R_s	Series resistance of the cell, ohm
$R_\square$	Sheet resistance, ohm/$\square$
R_s'	Equivalent series resistance, ohm-cm^2
t_{ox}	Oxide thickness, Å
t_F	Barrier metal film thickness, Å
T	Temperature, °K
$T(\lambda)$	Optical transmittance
V_{bi}	Zero bias band bending, V
V_{oc}	Open circuit voltage, V
ϵ_s	Semiconductor permittivity, F/cm
η	Efficiency of the solar cell
ν	Frequency of the radiation, sec^{-1}
ρ	Resistivity, ohm. cm
ϕ_B^p	Schottky barrier height, V
ϕ_M	Metal work function, eV
ϕ_s	Semiconductor work function, eV
χ_s	Semiconductor electron affinity, eV

SYNOPSIS

Schottky Barrier (SB) and Metal-Oxide-Semiconductor (MOS) solar cells have acquired considerable importance in recent years. However, some of the important questions related to the most suitable metal, optimum metal film thickness and interfacial oxide thickness in SB and MOS solar cells still remain unanswered. Aim of the present investigation was to find some of these answers.

Aluminium, chromium and tin have been studied as barrier metals on p-type silicon for SB/MOS solar cell applications. Cr and Sn devices made in the initial stage of the investigation indicated lower efficiencies as compared to Al devices. Moreover, chromium and tin thin films exhibited rapid degradation when exposed to air, resulting in a rapid degradation of device performance.

The optimum thickness of the Al film was found to be about 63 Å and the corresponding short-circuit current density was 25.2 mA/cm^2 without antireflection coating. The optimum interfacial oxide thickness seemed to lie in the range of 19 to 24 Å. The highest open-circuit voltage obtained without any ARC was 410 mV, the highest short-circuit current density 25.2 mA/cm^2, the highest fill factor 0.62, and the highest efficiency 4.05%. Very low values (R_s.Area = 0.07 $Ohm.cm^2$) of series resistance were obtained with Au back contact. Both

the value of n and the enhancement of diode current with light intensity increased with the oxide thickness. Under illumination the charge in interface states becomes more negative for p-type silicon, resulting in a higher oxide voltage and consequently a lower silicon band-bending. This increases the diode current and reduces somewhat the benefit of the interfacial oxide layer. The zero-bias silicon band-bending was found to increase with the oxide thickness. The increase in V_{oc} with oxide thickness can be partly explained by this and partly by the fact that the oxide potential barrier reduces the majority carrier diode current, however does not affect the minority carrier light-generated current, so long as the minority carrier tunneling time remains much smaller than their diffusion time through silicon.

CHAPTER - I

INTRODUCTION

One of the most promising of the alternative energy sources under current study is based on the direct terrestrial conversion of solar radiations to electrical energy via the photovoltaic effect using the solar cells.

1.1 SCHOTTKY BARRIER SOLAR CELL

Amongst the various types of solar cells under study, silicon Schottky Barrier Solar Cells (SBSC) have aroused considerable interest because of the following factors:

(i) They are surface barrier devices and therefore the depletion region in the semiconductor begins at the metal-semiconductor interface. This leads to higher collection efficiencies, specially at short wavelengths of light. This characteristic feature of SBSC's is of considerable significance when the minority carrier life time and diffusion length are small, as in the case of low-grade or polycrystalline semiconductors.

(ii) Because of fewer and simpler fabrication steps, processing cost of SBSC is low. Moreover, cells of any size and shape can be fabricated.

(iii) The Schottky barrier configuration can be extended to polycrystalline and amorphous semiconductors much more easily than the p-n junction configuration. An easier adaptability of the solar cell configuration to polycrystalline, amorphous and low-grade silicon is very much desired, since the use of these inexpensive materials will be an ultimate effort to reduce the cost/Watt of solar panels.

(iv) For SBSC, fabrication processes can be confined to low temperatures only and thereby the problem of degradation of minority carrier life time, associated invariably with high temperature processes, can be avoided.

The existing literature gives an account of the earlier Metal-Silicon surface barrier photocells developed by Mette (1958)[1], Mayer (1959)[2] and Gärtner (1962)[3]. However, these photocells were of extremely low conversion efficiencies but of considerable significance as they constituted the first step towards solid state high speed photo-detectors and α-particle detectors.

Almost a decade later, with the resurgence of interest in photovoltaics, the silicon Schottky barrier photo-cells have been investigated from the point of solar energy conversion. Theoretical[4] and experimental[5] work has

TABLE - 1.1

SUMMARY OF RESULTS REPORTED ON p-Si SB/MOS SOLAR CELLS

Orientation	ρ (Ω·cm)	Oxide Thickness (Å)	Barrier Metal	Area (cm^2)	V_{oc} (mV)	J_{sc} mA/cm^2	Fill Factor	Efficiency (%)	Reference
⟨100⟩ 30μ(EPI.)	2.2	10-15	50 Å Cr 50 Å Cu	1.5	530	22	0.65	7.6	(6)
⟨100⟩	2.0	10-15	50 Å Cr 50 Å Cu	1.04	520	30	0.60	9.5	(7)
-	3.5-15	20-40	Al (80-120 Å)	0.026	430	26.5	-	8.0	(8)
⟨100⟩	1.0	-	Au(70 Å)	0.019	400	40	0.63	10.5	(9)
⟨100⟩	1.0	-	Ti(50 Å)	2.6	550	33	0.65	11.7	(10)
⟨111⟩	-	-	Ti(50 Å)	2.5	500	32	-	8.0	(11)

1.3 PURPOSE AND SCOPE OF THE PRESENT INVESTIGATIONS

SB/MOS solar cells are comparatively new and still in the research stage. The efficient MOS solar cells reported by various workers[6-11] differ in barrier metal, interfacial oxide thickness, methods of growing oxide, cell geometry and crystal orientation. That makes their comparative assessment rather difficult. Hence, some of the questions like the most suitable metal, optimum metal film thickness, the best oxide growth technique, interfacial oxide layer thickness and the maximum efficiency possible, are still unresolved. Moreover, there is no experimentally verified explanation for the role of interfacial layers in SB/MOS solar cells and so their properties also need further investigations.

In our present investigation we have confined ourselves to the study of aluminium, chromium and tin as barrier metals. The scope of our investigation was to find out some of the questions related to the most suitable metal, optimum metal film thickness and interfacial oxide thickness for SB/MOS solar cells on p-type single crystal silicon.

1.4 CHOICE OF SEMICONDUCTOR

The choice of semiconductor material is dictated by two main factors namely efficiency and cost. Though GaAs is

the material with optimum efficiency (from band gap considerations)[14], silicon is the most widely accepted semiconductor for solar cell applications.

Silicon has the advantages of being:

(i) the most abundant solid element in the lithosphere;

(ii) a low cost, light weight, non toxic semiconductor of highly developed technology;

(iii) a high life time semiconductor with fairly good mobilities and therefore larger diffusion lengths, which aid collection of the photogenerated carriers;

(iv) a material with fairly low surface recombination velocity ($\sim 10^3$ cm/sec) so that recombination loss at the surface is small;

(v) a material that can be obtained easily in thin film form by techniques like vacuum deposition.

1.5 CHOICE OF METAL

One of the most important factors, which influence the performance of a SB/MOS solar cell, is the barrier metal. Unfortunately, there is a dearth of comparative assessment of various metals for this purpose. However, the barrier metal must meet the following requirements:

(i) The metal must be able to give a high barrier on p-type silicon.

(ii) It must exhibit good adherence to silicon and silicon oxide.

(iii) Thin metal films must be chemically and mechanically stable.

(iv) Its coefficient of thermal expansion should be close to that of silicon.

(v) Thin metal films must have high transmittance to sheet resistance ratio.

(vi) The metal should be easy to evaporate.

With the present day knowledge about metals, it is difficult to point out a metal which can meet all the requirements simultaneously.

To get a barrier on p-silicon the metal work function should be smaller than the semiconductor electron affinity (4.24 eV). To start with we have selected low work function metals Mg (3.19 eV), Sn (3.42 eV), Al (4.13 eV) and Cr (4.18 eV)[15]. From theoretical considerations $\left[\phi_{B}^{p} = E_g - (\phi_M - \chi_S)\right]$, Mg, Sn, Al and Cr are expected to give a barrier of 2.16, 1.94, 1.22 and 1.17 eV respectively, on p-type silicon[15]. Mg is expected to give the highest barrier on p-silicon but because of its relatively high vapor pressure, it should not be evaporated in the vacuum system where other metals are also to be evaporated.

The highest reported barrier height for Al-p silicon (MOS) contact is around 0.94 eV[16]. Chromium gives barrier

heights in the range of 0.7 eV[7] on p-silicon. Data for tin are not available.

Adherence of Al and Cr on silicon and silicon oxide is excellent, while that of Sn is poor and that of Mg is intermediate[17].

The reported transmittance of 75 Å thick Mg films is 50%[18], while that of Al and Cr films is only 30%[18]. However, transmittances of Al and Cr films can be increased from 30% to 70% by using suitable antireflection coatings[18].

The sheet resistance of 100 Å thick films of Al is around 10 ohms/□ as compared to 100 ohms/□ of Cr[19]. Data for Mg and Sn are not available.

Amongst all the metals, under study for SB/MOS solar cell applications, Al is a unique example. It not only exhibits excellent adhesion to silicon and silicon-oxide but it is easy to evaporate, in thin film (100 Å) form it is the third best electrical conductor[19], it is easily bondable and it is inexpensive and available in extremely pure forms.

In the course of our preliminary investigations we have studied Cr, Sn and Al SBSC's, while during later stages we have concentrated on Al-SB/MOS solar cells. They have been studied in some what greater details.

CHAPTER II

THEORY

2.1 PHOTOVOLATIC EFFECT

When light strikes a semiconductor, photons of sufficient energy (greater than the band gap of the semiconductor) break the covalent bonds to produce electron-hole pairs. These photo-generated carriers, which are in excess to the thermal equilibrium value, diffuse randomly in the semiconductor and recombine, unless they are separated by a built-in electric field in the semiconductor. A built-in electric field can be established in a semiconductor by variation of doping (as in case of p-n junction) or by deposition of a suitable metal on a semiconductor surface to form a Schottky barrier.

The separation of electrons and holes by a built-in electric field gives rise to photo-induced voltage (photovoltaic effect), while suitable electrical connections help in collection of charge carriers, giving rise to light generated current.

2.2 SCHOTTKY BARRIER SOLAR CELLS

When a metal with a work function ϕ_M is brought in an intimate contact with a semiconductor (say p-type) having

an electron affinity χ_S and work function ϕ_S, the Fermi levels in the two coincide at thermal equilibrium. If the metal work function is smaller than the sum of electron affinity and the band gap of the semiconductor, a barrier for holes is formed, cf. Figure 2.1(a). This barrier is commonly referred to as Schottky barrier. The limiting value of the barrier height (neglecting the Schottky lowering) is given by:

$$q \phi_B^p = E_g - (\phi_M - \chi_S) \qquad (2.1)$$

According to the simplest model, the built-in potential or zero bias band bending (V_{bi}) is given by the difference of the two work functions:

$$q V_{bi} = \phi_S - \phi_M \qquad (2.2)$$

The current transport in metal-semiconductor barrier, under low level injection condition, is mainly due to the majority carriers and the current-voltage relation is given by:

$$J = J_o \left[\exp(qV/kT) - 1 \right] \qquad (2.3)$$

J_o is the saturation current density and its value, from thermionic emmission theory, is given by:

$$J_o = A^{**} T^2 \exp(-q \phi_B^p / kT) \qquad (2.4)$$

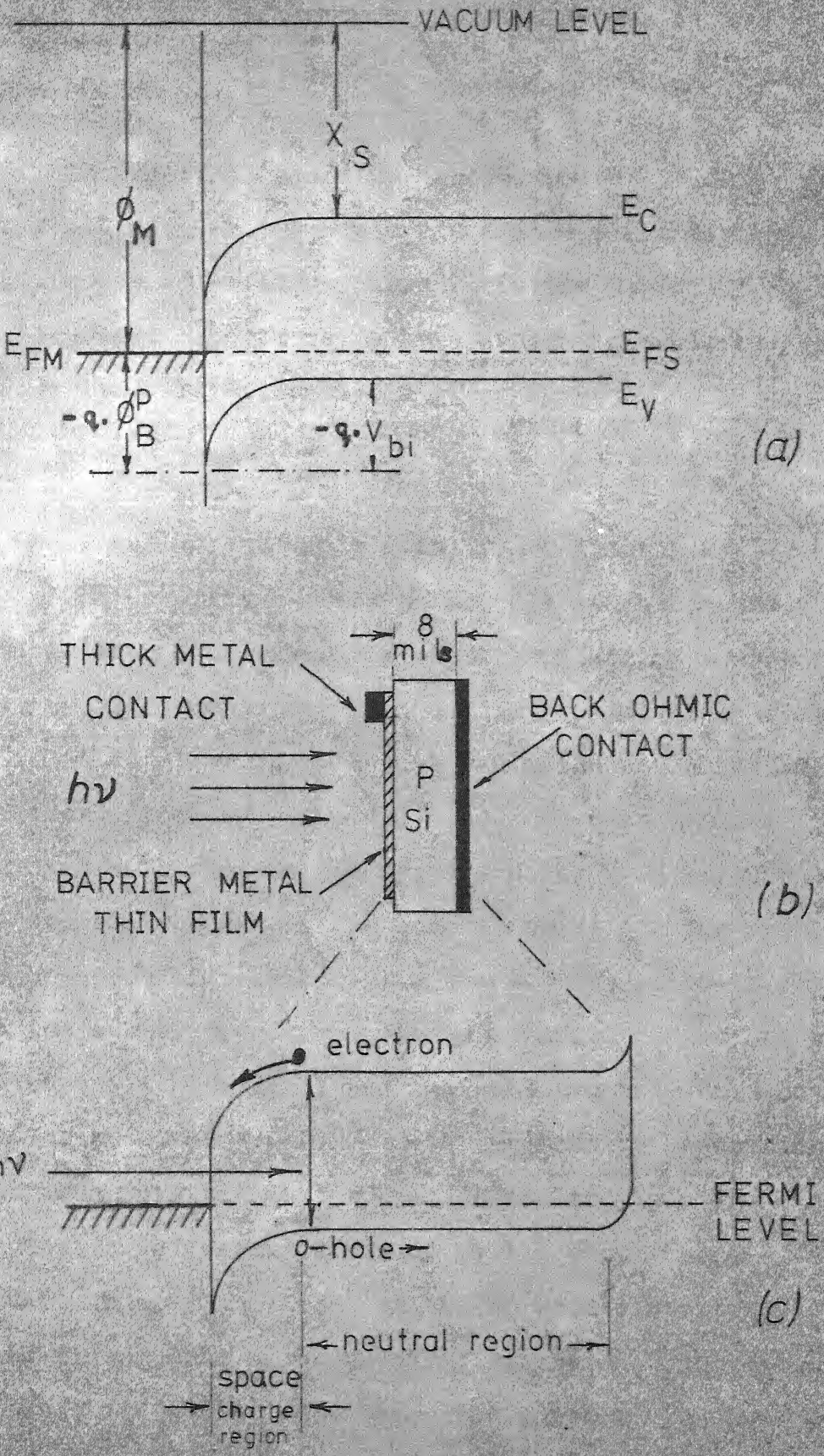


FIG. 2.1. STRUCTURE AND BAND DIAGRAM OF AN S B S C

In practical Schottky diodes, however, due to the presence of inevitable surface states and the interfacial oxide, the current-voltage characteristics deviate from the ideal behavior. Therefore, a more general expression for current-voltage relationship is given by:

$$J = J_o \left[\exp(-qV/nkT)-1 \right] \qquad (2.5)$$

where, n is called the diode ideality or quality factor.

The Schottky barrier solar cell can be looked upon as a large area Schottky diode with a difference that the barrier metal is deposited in the form of semitransparent thin film, so as to allow the incident radiation to be absorbed in the semiconductor, cf. Figure 2.1(b). When an SBSC is illuminated with photons of energy greater than the band gap of the semiconductor, the absorption of photons results in the creation of electron-hole pairs. The built-in field drifts the two types of carriers in opposite direction, namely the electrons to the metal and the holes to the semiconductor (p-type) region, cf Figure 2.1(c). The charge separation results in a potential difference across the barrier. However, this potential difference, set up by the photogenerated electron-hole pairs, biases the diode in the forward direction, with the effect that a current I_D flows through the diode.

If I_L is the light generated current, the current I, which flows through an externally connected load is given by:

$$I = I_L - I_D \qquad (2.6)$$

Short circuit current

When the external load is shorted, the voltage across the solar cell and hence the diode current (I_D) drops to zero. Under this condition and assuming the series resistance of the cell to be zero, the short circuit current becomes equal to the light generated current, cf. Figure 3.2(a).

or $$I_{SC} = I_L \tag{2.7}$$

Open circuit voltage

When the external load is zero, maximum voltage appears across the diode. This voltage is known as the open circuit voltage (V_{oc}) cf. Figure 3.2(b). Under this condition, the diode current becomes equal to the light generated current.

$$J_L = J_D = J_o \left[\exp (qV_{oc}/nkT)-1 \right] \tag{2.8}$$

or

$$V_{oc} = n \left[\phi_B^p - \frac{kT}{q} \ln \frac{A^{**} T^2}{J_L} \right] \tag{2.9}$$

Equation (2.9) shows the dependence of the open circuit voltage on the barrier height and the ideality factor of the diode.

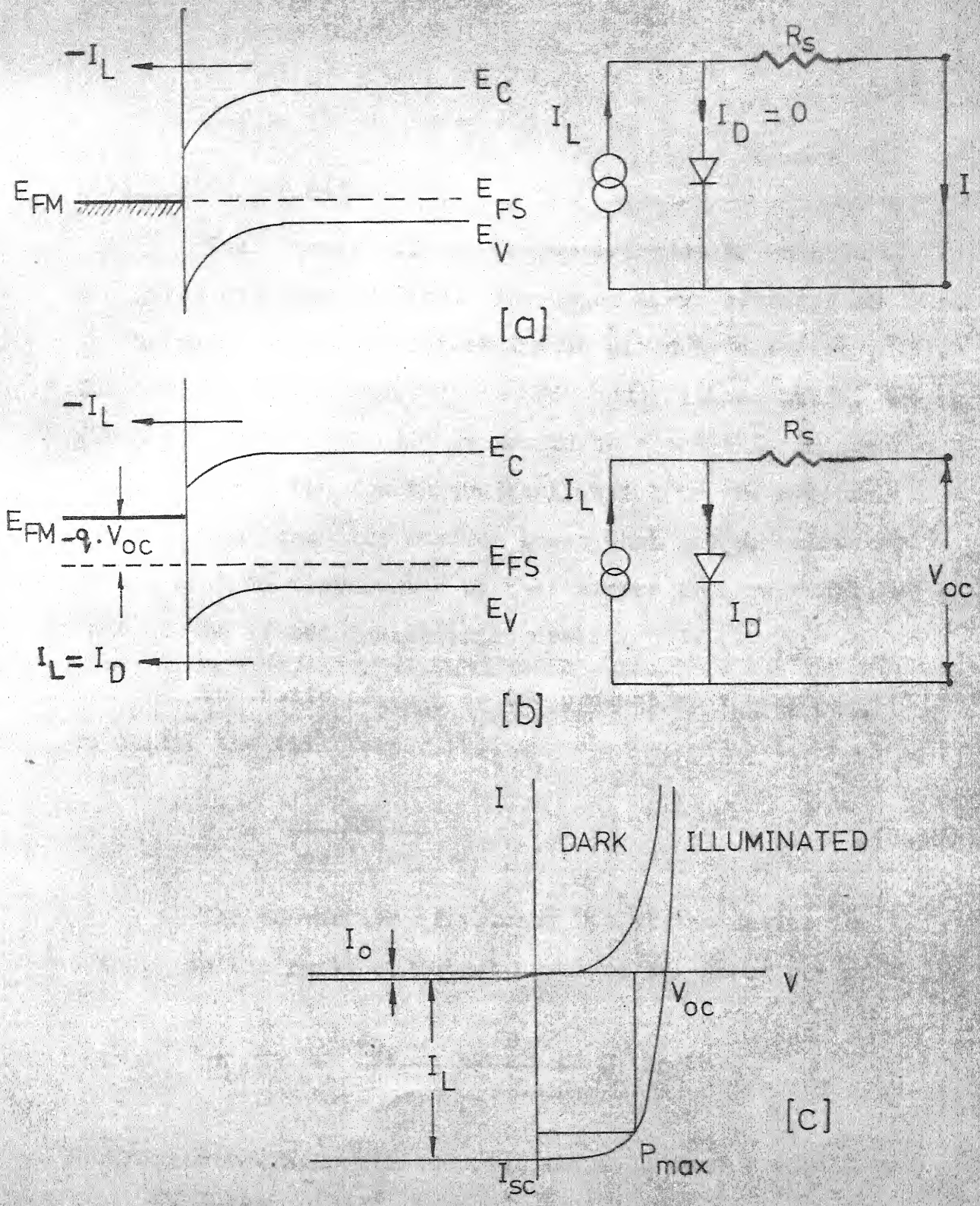


FIG. 2.2 . ENERGY BAND DIAGRAM OF AN SBSC UNDER ILLUMINATION AND:

[a] SHORT CIRCUIT CONDITION

[b] OPEN CIRCUIT VOLTAGE CONDITION

[c] DARK AND ILLUMINATED I-V CHARACTERISTICS OF AN SBSC .

Fill factor and efficiency

The current-voltage characteristics of an SBSC are given in Figure 2.2(c). The upper curve corresponds to the dark diode I-V characteristic given by equation (2.5). The lower curve corresponds to SBSC under illumination, and is given by equation (2.6). It should be noted that this curve passes through the fourth quadrant, which is the region of power generation. The maximum power that can be delivered by the cell is represented by the largest area rectangle that can be fitted inside this curve.

The ratio of P_{max} to the product of V_{oc} and J_{sc} is called the fill factor (F).

$$F = \frac{P_{max}}{V_{oc} \cdot J_{sc}} \tag{2.10}$$

The conversion efficiency (η) of the device is defined as the ratio of output power to the input power (P_{in}).

$$\eta\ (\%) = \frac{J_{sc} \cdot V_{oc} \cdot F}{P_{in}} \times 100 \tag{2.11}$$

For high conversion efficiencies the fill factor should be close to unity.

Series resistance

In an SBSC, the series resistance originates from the semiconductor bulk and the metalized contacts. This

series resistance being a parasitic parameter, affects the efficiency of the cell by reducing the fill factor and the short circuit current. The resistance has got more pronounced effect on the fill factor, e.g. it has been observed that a series resistance of 5 ohms can reduce the fill factor of an SBSC (1 cm^2 area) from 0.67 to 0.42[7]. Therefore, it is very essential to keep the series resistance low.

2.3 DESIGN CONSIDERATIONS IN SILICON SBSC.

The ultimate conversion efficiency of an SBSC is limited by certain physical phenomenon, such as quantum loss and other considerations pertaining to the material and geometry of the system.

Silicon resistivity

In an SBSC, the collection efficiency is expected to improve with greater space charge region width. This requires a low doping concentration in the semiconductor, which in turn increases the bulk resistivity and hence the series resistance. Moreover, for a better collection efficiency, the minority carrier diffusion length is desired to be large, so that the carriers which are generated in the neutral region of the semiconductor are also collected.

On the other hand, the doping level in the semiconductor should be large, in order to reduce the semiconductor resistivity

and hence the series resistance. A high doping density affects the minority carrier life time and the diffusion length. Moreover, a high doping density gives rise to large reverse saturation current, which is undesirable. Therefore, an optimization of doping level is necessary. The optimum doping concentration for silicon is 10^{15}-10^{16} cm^{-3}, which corresponds to 1-10 ohms cm resistivity[20].

Film thickness

The optimum thickness of the barrier metal film is obtained from optical and electrical considerations. Maximum transmission of the incident radiation through the metal film requires low reflection from the metal surface and low absorption in the metal film. The reflection losses can be minimized by the use of proper anti-reflection coatings. Absorption within the film can be minimized by having very thin films. But this gives rise to discontinuity and large sheet resistance, leading to large value of series resistance. The thickness of the film should be optimized such that the transmittance to sheet resistance ratio is maximum[21]. For better collection and lower series resistance, optimized grid structure is generally used.

2.4 ROLE OF INTERFACIAL LAYER IN SCHOTTKY DIODES AND SOLAR CELLS

When a metal contact is evaporated on a chemically prepared silicon surface, the metal and semiconductor are never in an intimate contact. An interfacial layer of atomic dimensions inevitably separates the two.

The presence of interfacial film affect the properties of Schottky diodes in several ways:

(i) A potential barrier is presented by the energy gap of the layer, to the mobile carriers in silicon.

(ii) A potential difference can sustain, between the metal and the semiconductor, at the interface. This potential is bias dependent and gives rise to reduced dependence of the semiconductor surface potential on the applied bias.

(iii) The built-in potential in the semiconductor is altered by the presence of insulator.

(iv) The interface state density decreases with increasing oxide thickness[22].

(v) The charging of the interface takes place by charge tunneling between these states and metal or by interaction with the carriers in the semiconductor by recombination/generation, depending on the oxide thickness[23].

When an interfacial layer is not present (as in case of vacuum cleaved silicon surface), due to a large number of interface states, communicating with the metal, it is said that the metal Fermi level is pinned to the interface states. As the oxide thickness increases, say up to 10 Å, the diodes behave basically the same way as the ideal Schottky barrier, except for the fact that the zero bias barrier height may be lower (~ 0.55 eV for Al-p silicon)[13]. Most of the real life metal-silicon contact diodes come under this category. It has been observed that with further increase in oxide thickness, the barrier height of aluminium-p silicon contact increases monotonically[8,22]. Moreover, with thicker oxides, a greater proportion of interface states communicate more readily with semiconductor, leading to higher values of n.

Equation (2.9) suggests that the open circuit voltage of an SBSC can be increased either by using higher barriers at the metal semiconductor contact or by increasing the diode ideality factor (n).

Experimentally it has also been verified that by introducing thicker interfacial oxide layer and thereby increasing the value of n, the open circuit voltage can be increased considerably[24-26].

The large increase in the open circuit voltage of an SBSC, due to increase in the interfacial oxide thickness

can be mainly due to many orders of magnitude drop in the diode current (majority carrier current) whereas the light generated (minority carrier) current remains unaffected up to some limiting value of oxide thickness. It has been proposed that an interfacial layer can be designed such that it is not efficient in the transport of majority carriers while completely transparent to the minority carriers[27].

Several theories[22,27-30] have been put forward to explain the role of interfacial layer in an SBSC. One explanation given by Fonash[27] is based on the considerations that when a SBSC is illuminated a part of the developing voltage appears across the semiconductor and the rest across the interfacial layer. Since the total developing voltage does not appear across the semiconductor the majority carrier (diode) current is reduced due to a less reduction in the band bending. For a given developing voltage, a larger current is produced then would be if there is no interfacial layer. This improves the efficiency of a solar cell.

On the basis of investigations on silicon MOS tunnel diodes, Kar[22,28] has shown that thicker oxides not only increase the oxide barrier, but silicon barrier as well, due to a large reduction in interface state density. The diode current due to majority carriers is always affected and reduced by the combined effect of increased V_{bi} and tunneling time, whereas the light generated current is

affected only when tunneling time becomes larger (due to increased oxide thickness) than the time it takes the minority carriers to diffuse to the interface.

Figure 2.3 shows an MOS solar cell under short circuit condition. τ_g is the minority carrier generation time, τ_i is the time minority carriers take to diffuse to the interface and τ_T is tunneling time.

Card and Yang[30] have put an argument that increase in open circuit voltage of MIS Schottky solar cells can be understood by taking proper account of the behavior of the interface states under the illuminated condition. Interface states in a solar cell communicate most readily with minority carriers and as a result act to reduce the potential drop in the interfacial layer, in contrast to their effect in dark forward-biased diodes. Under illumination, occupancy of the states changes, so band bending and current change. They argue that the increase in the open circuit voltage cannot be explained in terms of an increased value of n, for the dark current. Instead, they derive an expression for V_{oc} from the effect of the interfacial layer on tunnel transmission coefficient for the majority carriers. An optimum thickness of 20 Å is predicted for interfacial layer, above which it behaves like a simple series resistance. Upto thickness of 20 Å for the oxide, the light generated current

remains unaffected while V_{oc} increases monotonically. Beyond a thickness of 20 Å V_{oc} and J_{sc} both drop rapidly.

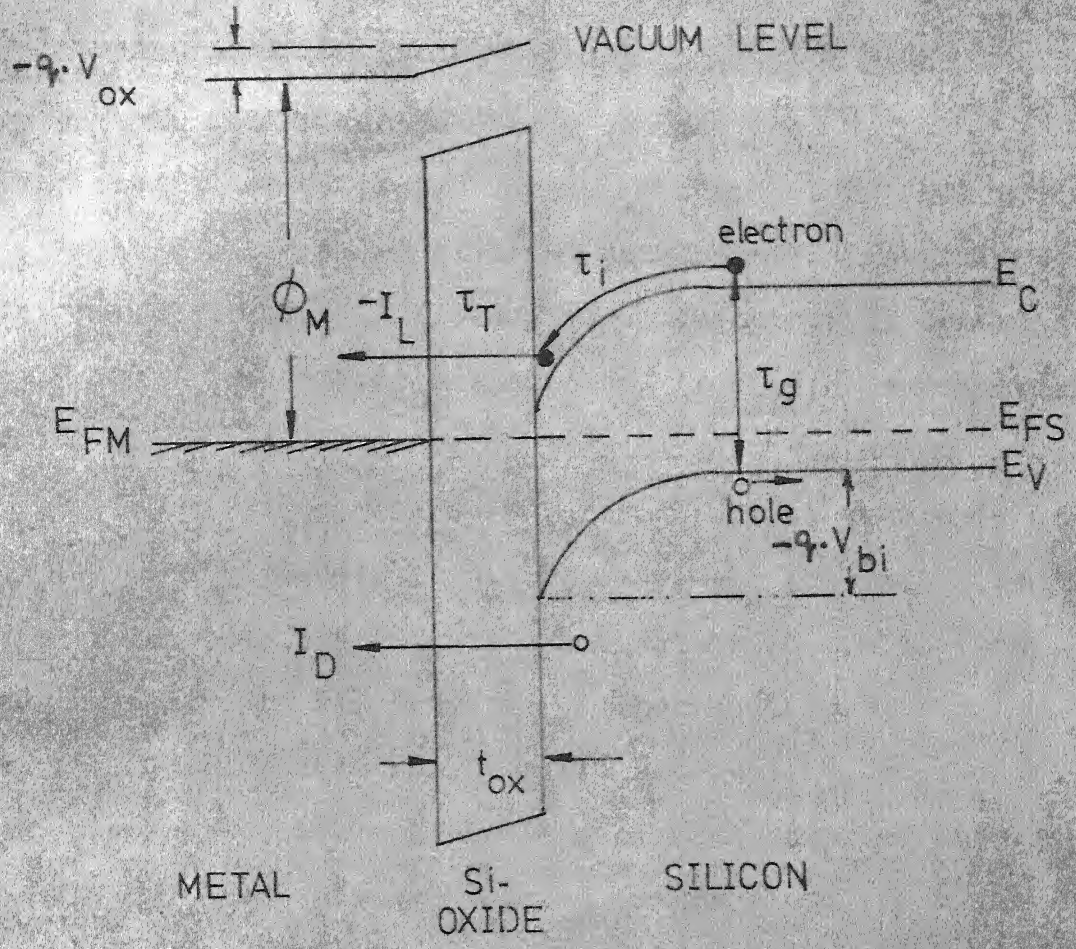


FIG.2.3 MOS SOLAR CELL UNDER ILLUMINATION
[SHORT CIRCUIT CONDITION]

CHAPTER III

FABRICATION AND CHARACTERIZATION OF THE DEVICES

3.1 FABRICATION FACILITIES

All modern semiconductor devices need to be fabricated very carefully and in an ultra clean environment, because of their small size and extreme susceptibility to contamination. In a clean room the particle count is kept below a specified maximum and air flow, temperature, humidity and air pressure are regulated. For semiconductor device fabrication, class 100 clean space is generally recommended (Appendix III). However, the laboratory facility accesible to us consists of a semi-clean room with air-conditioners and air blowers. Proper sealing of windows make it dust free to a reasonable extent. The most critical processes like chemical cleaning of semiconductor wafers, metals and filaments are carried out on class 100 clean benches. The other facilities include, diffusion, oxidation and annealing furnaces, vacuum coating units, photo-lithography room, ultrasonic bonding machines and deionized water plant.

3.2 FABRICATION PROCESSES

The processes involved in the fabrication of SB/MOS solar cells are:

(i) Surface cleaning of silicon, metals and filaments.

(ii) Oxidation of silicon (for MOS solar cells).

(iii) Metalization of silicon by vacuum evaporation techniques.

3.2.1 SURFACE CLEANING PROCESSES

The surface cleaning of the filaments, metals and semiconductor wafers was done as described below.

(a) Cleaning of filaments and metals

The cleaning procedure adopted is same for all filaments and metals. They were only degreased in organic solvents.

First they were rinsed in boiling trichloroethylene (TCE), to remove the organic impurities. Then they were rinsed in boiling acetone to remove the traces of residual TCE. Finally they were cleaned with warm methanol to remove the traces of acetone completely. Metals and filaments were not etched in any acid, as they were received in a clean state and as it becomes rather difficult to remove the traces of an acid from the metal surfaces.

(b) Cleaning of silicon wafers

The following procedure, in sequence, was adopted to clean the silicon wafers.

(i) Silicon wafer was put in a low sodium content pyrex beaker and degreased by boiling in TCE for 3-4 minutes.

(ii) Traces of TCE were removed by treating the wafer with warm acetone.

(iii) To remove the traces of acetone, the wafer was then rinsed with warm methanol.

(iv) The wafer was then thoroughly rinsed in deionized water to remove all the traces of methanol.

(v) Then it was transferred into a clean teflon beaker and treated with HF for two minutes, to remove 30-40 Å thick native silicon oxide.

(vi) The wafer was decanted in deionized water 8 to 10 times to remove HF completely.

(vii) 50-60 Å thick oxide was grown on silicon wafer by treating it with HNO_3 for one minute.

(viii) In order to remove the traces of HNO_3, it was decanted in deionized water about 8-10 times.

(ix) The grown oxide was then etched by treating the wafer with HF for 3 minutes.

(x) The wafer was finally rinsed in DI water thoroughly.

After this chemical cleaning silicon wafer should be hydrophobic (test) otherwise the whole procedure should be repeated. Steps (VII.) to (IX) were employed to remove minor mechanical defects and some of the diffused impurities at the surface.

3.2.2 OXIDATION OF SILICON

It has been observed that when freshly etched silicon surface is exposed to room air, about 10 Å thick film grows on its surface, immediately. However, at room temperature further growth of oxide takes place at very slow rate e.g. it takes one day to grow another 10-11 Å of oxide (Appendix I).

For the fabrication of SBSC's, silicon wafers were transferred to the vacuum chamber immediately after the chemical cleaning. For MOS solar cells, room temperature grown natural oxide and HNO_3 grown oxide had been employed.

3.2.3 VACUUM EVAPORATION OF METALS

Metalization for an SBSC, by vacuum evaporation techniques, includes:

(i) Deposition of thin (50-120 Å) semitransparent film of the barrier metal on the front (polished) surface.

(ii) Deposition of thicker film (preferably of the same metal) for making a pad for the front contact probe and for better collection.

(iii) Deposition of metal on the unpolished back surface of the wafer for ohmic contact.

Deposition of barrier metal thin films is one of the most critical steps in the fabrication of SB/MOS solar cells, since the properties of the films govern the performance of these devices. Therefore, the evaporation should be performed at minimum possible pressure (preferably below 10^{-5} torr).

After surface cleaning, the filament was fired in vacuum. The firing was done at a temperature higher than the evaporation temperature of the metal to be evaporated. This precautionary step eliminates the chances of degassing of the filament during actual evaporation and subsequent contamination of the metal.

Cleaned metal and silicon wafer were loaded in the vacuum chamber and with the help of properly alligned Al/Mo masks front contacts were made.

TABLE 3.1

EVAPORATION DATA OF METALS

Metal (Purity)	Filament Source	Evaporation Temperature (°C)
Al (99.999%)	W-helical coil	1217
Au (99.99%)	W-helical coil	1397
Cr (99.99%)	W-conical basket	1397
Sn (99.999%)	W-conical basket Mo-holder	1250

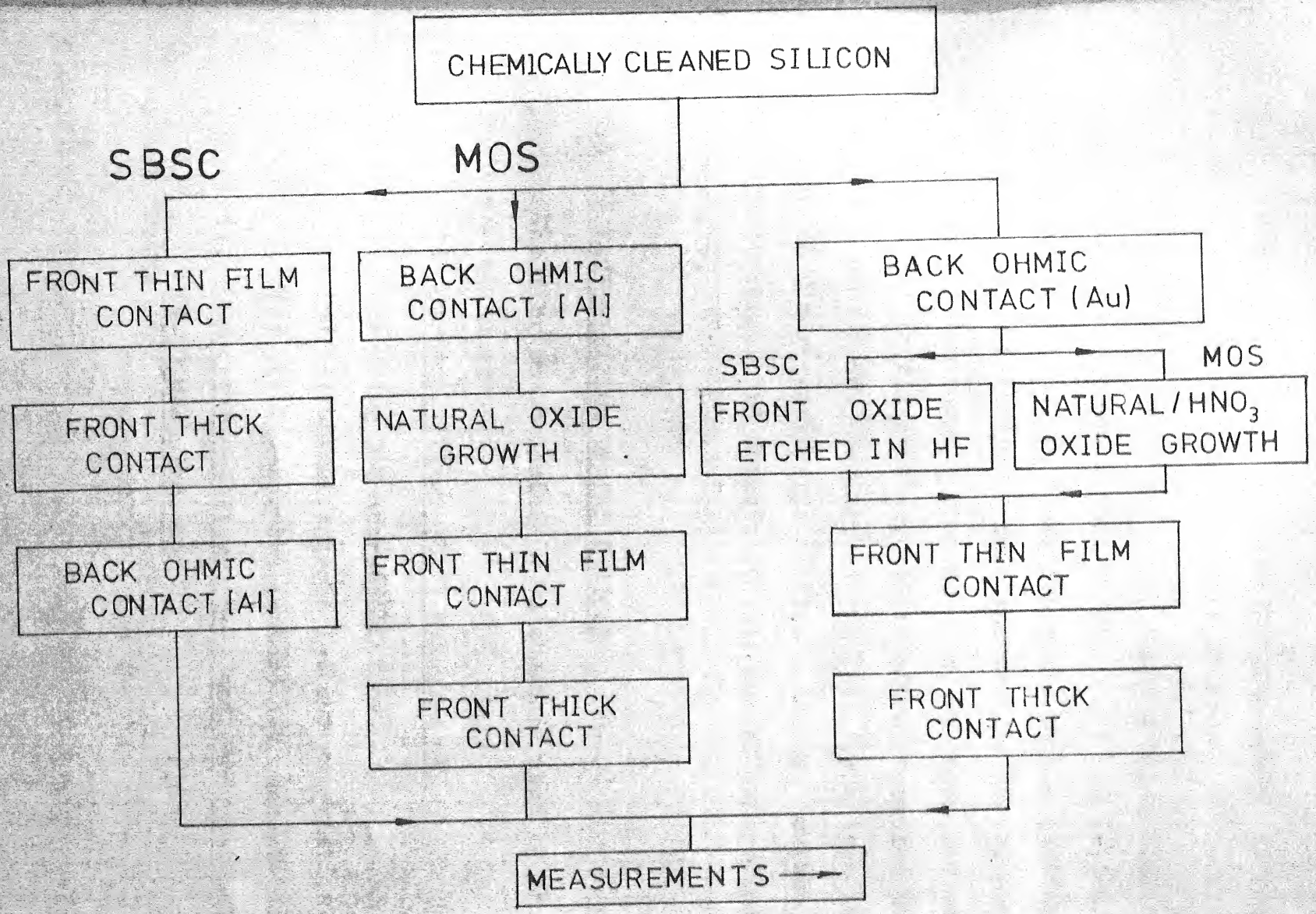


Fig. 3·1

SEQUENCE OF STEPS FOLLOWED FOR THE FABRICATION OF SOLAR CELLS

Chart of Figure 3.1 shows the sequence of fabrication steps followed for SB and MOS solar cells.

The initial devices were fabricated using Hind Hivac 12A4 vacuum coating unit. Later, all the devices were fabricated using more sophisticated vacuum coating unit (Grainville and Phillips). Both the systems employ rotary and oil diffusion pumps. Therefore, to minimize oil vapor contamination in the chamber, liquid nitrogen cooled baffles and traps were used. Grainville and Phillips system includes Perkin and Elmer quartz crystal film thickness monitor and so film thickness and deposition rate can be controlled accurately.

3.3 CHARACTERIZATION OF THE DEVICES

The fabricated devices were characterized by the following measurements.

(i) Current-Voltage (I-V) Measurements

(a) Dark I-V characteristics.

(b) Illuminated diode I-V characteristics.

(c) Photogenerated (solar) I-V characteristics.

(ii) Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) Measurements

For the purpose of measurements, back and front electrical contacts to the device were made by mounting it on a gold plated copper block and using a light pressure, palladium coated brass probe with telescopic spring.

Sun light was simulated in the laboratory with a coiled coil tungsten filament lamp. The radiation level was adjusted at 100 mW/cm^2 (AMI) with the help of a calibrated p-n junction solar cell (Appendix IV).

Dark I-V Characteristics

The circuit for making the measurements is shown in Figure 3.2(a). These measurements yield information regarding the ideality factor (n) in dark, reverse saturation current (I_o) and the series resistance. The n-value at any point is determined from the slope of the tangent at the point when lnI is plotted against V.

$$n = \frac{q}{kT} \cdot \frac{\partial V}{\partial (\ln I)} \qquad (3.1)$$

The reverse saturation current can be determined using the log I-V characteristics of the reverse biased diode. It is given by the intercept on the current axis which is obtained when the linear part of the curve is extrapolated to intersect the current axis.

Illuminated Diode I-V Characteristics

The characteristics are computed from the measured current-voltage characteristics of the device under AMI illumination, with an applied bias, cf. Figure 3.2 (a), using the relation $I_D = I_L - I$. The characteristics yield the n-values under illumination, and open circuit voltage.

Photogenerated (solar) I-V Characteristics

The circuit for the measurement of solar I-V characteristics is shown in Figure 3.2(b). The measurements, taken under AMI intensity, give the actual power generation capacity of a solar cell by yielding V_{oc}, J_{sc} and the fill factor (F). The efficiency in percentage of a solar cell is computed from:

$$\eta = \frac{V_{oc} \cdot J_{sc}}{P_{in}} \cdot F \times 100 \qquad (3.2)$$

C-V and G-V Characteristics

The C-V and G-V measurements were taken using a fixed frequency (100 kHz) capacitance bridge, Boonton model 74 C-S 18, as shown in Figure 3.2 (c). When $1/C^2$ is plotted agains the bias voltage, the intercept of the

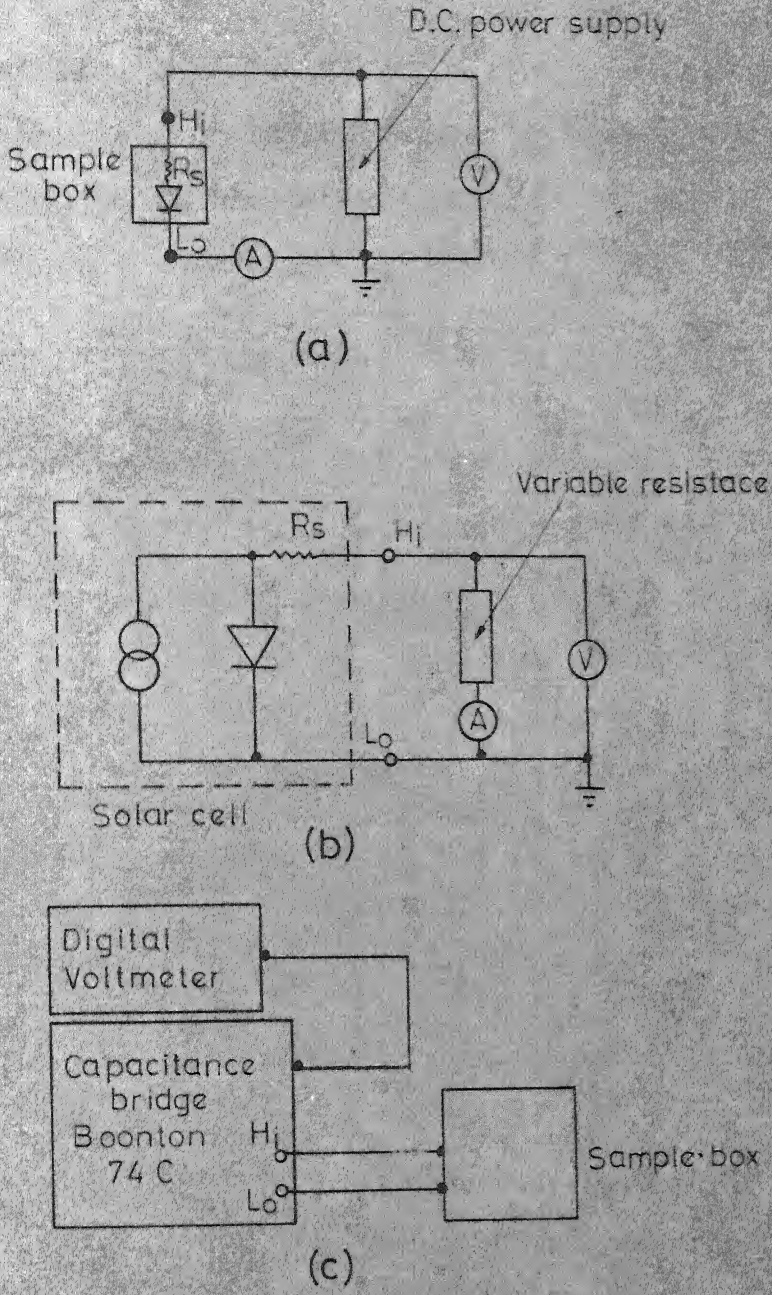


FIG. 3.2 SCHEMATIC CIRCUIT DIAGRAM FOR

(a) Current-voltage measurements

(b) Photogenerated current-voltage measurements

(c) Capacitance-voltage and conductance-voltage measurements

straight line on voltage axis, gives the built in potential of the barrier and the slope of the line gives the doping concentration in the semiconductor. For a p-type semiconductor:

$$N_A = \frac{2}{q \epsilon_S} \cdot \frac{\partial V}{\partial (1/C^2)} \qquad (3.3)$$

CHAPTER-IV

RESULTS AND DISCUSSION

4.1 BACK OHMIC CONTACT

The back ohmic contact in a solar cell has to be such that it does not limit the majority carrier current and that the voltage across the contact is negligible.

There are three major approaches to achieve an ohmic contact: (1) by choosing a metal with proper work function so that barrier is small for thermally excited carriers, (2) by heavily doping the semiconductor near the junction, so that the carriers can be transported by quantum mechanical tunneling, and (3) by introducing numerous recombination centers in the interface region (on the semiconductor side of the junction). Another simple approach, for making ohmic contact on p-silicon, employs alloying of aluminium with silicon to form a heavily doped p^+ region.

In the beginning, we used aluminium for back ohmic contact. It was thought that, since large number of recombination centers are presented on the back unpolished surface of commercially available silicon wafers, any low resistivity metal should be able to give a good ohmic contact. However, very soon it was realized that the fill factors of the devices

with Al-back contacts were poor (F ~ 0.35) mainly due to high series resistance originating from the back contact. In order to make an intimate contact, aluminium was then alloyed with silicon. But due to unavailability of pure nitrogen, alloying technique was discontinued.

After Al, several other metals including copper, silver, indium and gold were tried for ohmic contacts. Since, gold has the highest work function (5.06 eV)[15] it is expected to give the best ohmic contact on p-silicon. Gold indeed exhibited the best ohmic contact on p-silicon and hence it was selected for making further ohmic contacts. Gold proved to be very suitable as with gold back contact it was possible to etch the front oxide without affecting the back contact.

In an effort to reduce the series resistance further, p/p+ (ρ = 1.04 Ω cm) epitaxial wafers (MONSANTO) were used. These epitaxial wafers were found not very suitable since the solar cells exhibited poor short circuit current, due to small thickness (9 microns) and low minority carrier lifetime of the epitaxial layer. The series resistance obtained with the above epitaxial wafers was around 6 ohms for a cell with an area 0.023 cm^2.

4.2 CHROMIUM AND TIN DEVICES

Chromium and tin devices were fabricated on polished (111) p-silicon wafers having resistivity in the

range of 0.2-1 Ohm.cm. Thin film dots (1mm Ø) and thick contact dots (1/2 mm Ø) were obtained with the help of molybdenum masks. Aluminium was deposited on the back unpolished surface for ohmic contact.

Since, chromium does not melt easily (m.p. 1900°C), but sublimes during evaporation, it was taken in the form of small pellets. Even then, evaporation of a small amount of chromium required the filament to be maintained at high temperatures for considerably long durations (10-15 minutes). This posed a severe problem of overheating of the vacuum chamber with subsequent degassing and difficulty in maintaining the pressure below 10^{-4} torr. Similar problems of excessive heating and degassing were posed by tin also.

The chromium and tin SBSC's, so fabricated, exhibited low open circuit voltages and short circuit currents and poor overall conversion efficiencies. Moreover, chromium and tin thin films exhibited rapid degradation (fogging and flaking of films) when exposed to air, resulting in a rapid degradation of device performance. Table 4.1 summarises the results obtained with chromium and tin contacts.

The reason for observed low short circuit current can be attributed to rapid degradation of the thin films. The observed low open circuit voltages and high reverse saturation currents are mainly due to low barrier heights

Table 4.1

Characteristics of Cr and Sn SBSC's

Device	Metal	$T(\lambda)^*$ (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	ϕ_B^p (from I-V) (eV)
4	Cr	21	60	3.70	0.41
14	Sn	32	70	0.59	0.44
15	Sn	20	110	0.45	0.51
16	Sn	12	70	3.00	0.48
18	Cr	85	105	1.30	0.43

* WHITE LIGHT TRANSMITTANCE OF FILMS DEPOSITED ON GLASS

obtained. The barrier heights may be low either due to contamination of metal or silicon surface, as a result of excessive degassing, or due to the fact that high temperature evaporation can result in the penetration of metal atoms into the silicon surface.

The low barrier heights observed in the case of chromium SBSC's agree with the observations of Anderson[4]. It has been reported that evaporated chromium-p-silicon diodes exhibit barrier heights in the range 0.35 - 0.39 eV, whereas sputtered-chromium diodes show a barrier in the range 0.82 - 1.00 eV[4]. Data for Sn are not available.

4.3 ALUMINIUM DEVICES

In the beginning, aluminium SBSC's were fabricated on 0.2-1 ohm cm (111) silicon polished wafers. Front thin film dots (1 mm ø) and thick contacts (1/2 mm ø) were deposited at the rate of 5-10 Å/second. The pressure during evaporation was always maintained below $2X10^{-5}$ torr.

Later, larger area cells were also fabricated and parameters like resistivity and aluminium film thickness were varied to see their effect on the device performance.

For the purpose of MOS solar cells, oxide was grown at room temperature by storing the back metalized silicon wafers in a clean space. An account of the room air exposure time was kept, for the estimation of oxide thickness. Oxide was also grown by treating the wafer in HNO_3 at room temperature.

Tables 4.2 to 4.4 summarize the experimental results obtained. The I-V characteristics of these devices are included in Figures 4.1 to 4.10.

OXIDE THICKNESS

The values of oxide thickness in MOS devices can be obtained by using their capacitance-voltage characteristics in strong accumulation. However for $t_{ox} > 20$ Å, the d.c. conductance of the diode becomes too large[23, 28]. This makes

TABLE 4.2

CHARACTERISTICS OF Al SB/MOS SOLAR CELLS

Device	ρ Ohm.cm	t_{ox} (Å)	t_F (Å)	T(λ) (%)	Total area (mm^2)	Effective area (mm^2)	V_{oc} (mV)	J_{sc} (mA/cm^2)	F	η (%)	R_s Ω	R'_s Ω.cm^2
74	3-7	13.5*	63	34	3.14	2.36	220	25.20	0.62	3.44	4	0.13
22	0.2-1	16.0*	135	8	9.00	6.00	300	6.65	0.60	1.20	15	1.35
2[illegible]	3-7	18.5*	48	55	0.79	0.59	410	10.00	0.45	1.85	240	1.87
8	0.2-1	23.5*	71	28	0.79	0.59	370	20.30	0.53	4.05	300	2.37
6[illegible](c)	4-12	26.5*	54	42	9.10	8.32	340	19.40	0.53	3.50	20	1.82
6[illegible](a)	3-7	30.0*	59	38	4.00	4.00	343	6.80	0.28	0.65	1.2K	48.00
23†	0.2-1		135	8	0.79	0.59	400	5.10	0.56	1.15	9	0.07

* Tolerance ± 2 Å

† HNO_3 grown oxide

Maximum probable error in the measurement of efficiency ± 8%

T(λ) computed from earlier results[19] (see Appendix II).

TABLE 4.3

CHARACTERISTICS OF Al SB/MOS SOLAR CELLS

Device	t_{ox} Å	J_o A/cm^2	ϕ_B^p V	Value of n					
				At 100 mV		At 200 mV		At 300 mV	
				Dark	Illuminated	Dark	Illuminated	Dark	Illuminated
74	13.5	2.2×10^{-5}	0.65	1.04	-	1.33	1.30	3.16	3.16
22	16.0	8.9×10^{-6}	0.68	1.58	1.25	1.58	1.25	1.58	-
28	18.5	-	-	2.50	2.50	3.92	3.92	7.50	7.50
8	23.5	-	-	1.80	-	2.50	2.25	3.00	2.90
66(c)	26.5	-	-	2.08	2.83	2.25	7.40	3.42	11.50
68(a)	30.0	-	-	2.58	3.92	3.75	5.25	4.40	6.80
23	-	-	-	1.58	-	1.91	1.84	2.58	2.56

TABLE 4.4

Data of SB/MOS solar cells obtained from $1/C^2$ - V characteristics

Device	t_{ox} Å	N_A (from ρ) cm^{-3}	N_A (From $1/C^2$-V) cm^{-3}	V_i V	ϕ_p V	ϕ_B^{p*} V	V_{oc} mV
74	13.5	2.0×10^{15} - 5.0×10^{15}	4.3×10^{15}	0.50	0.20	0.73	220
22	16.0	1.6×10^{16} - 1.5×10^{17}	3.2×10^{16}	0.56	0.15	0.74	300
28	18.5	2.0×10^{15} - 5.0×10^{15}	7.1×10^{15}	0.69	0.19	0.91	410
8	23.5	1.6×10^{16} - 1.5×10^{17}	5.9×10^{16}	0.70	0.13	0.85	370

$$\phi_p = E_{FS} - E_V$$

$$\phi_B^{p*} = V_i + \frac{kT}{q} + \phi_p$$

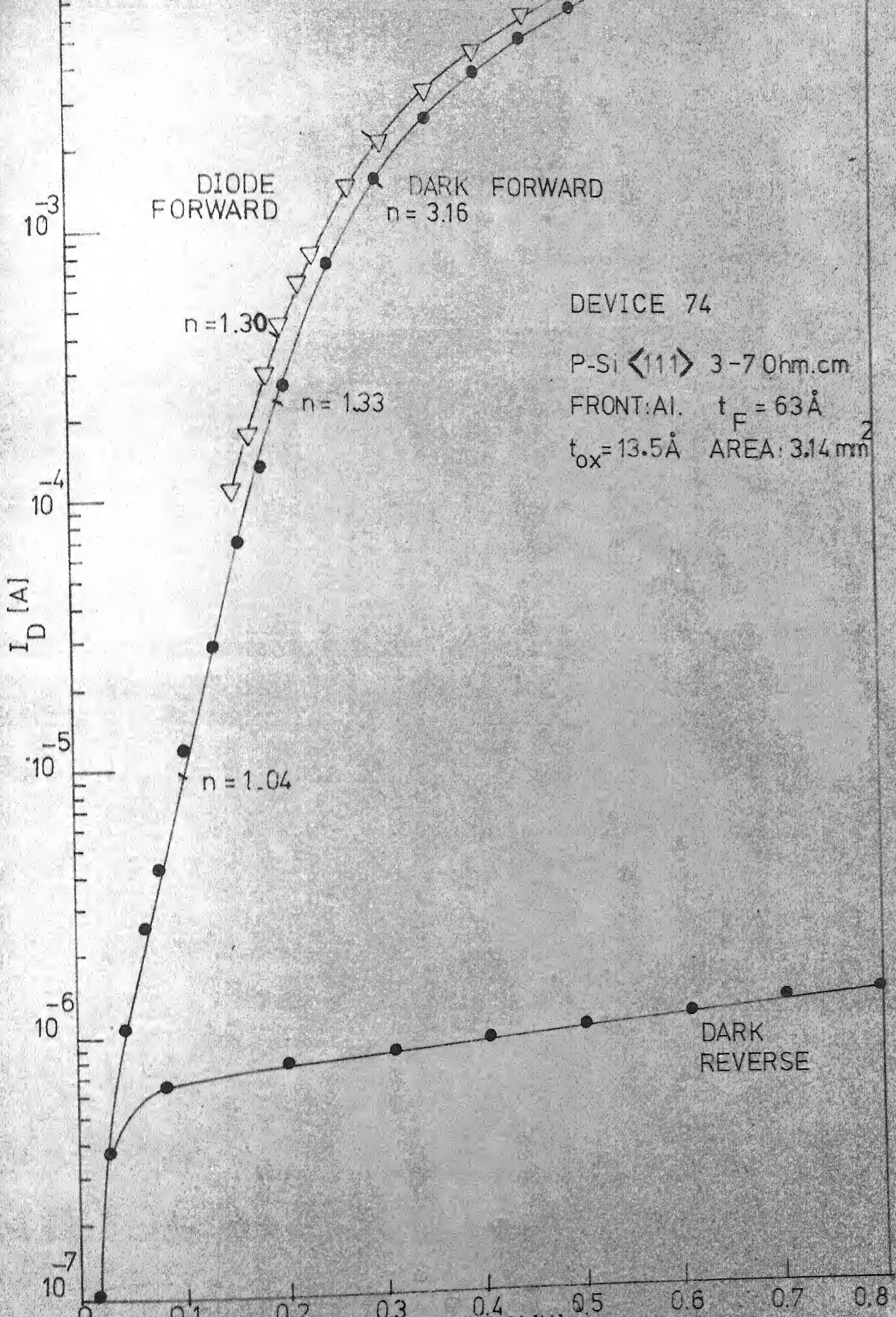
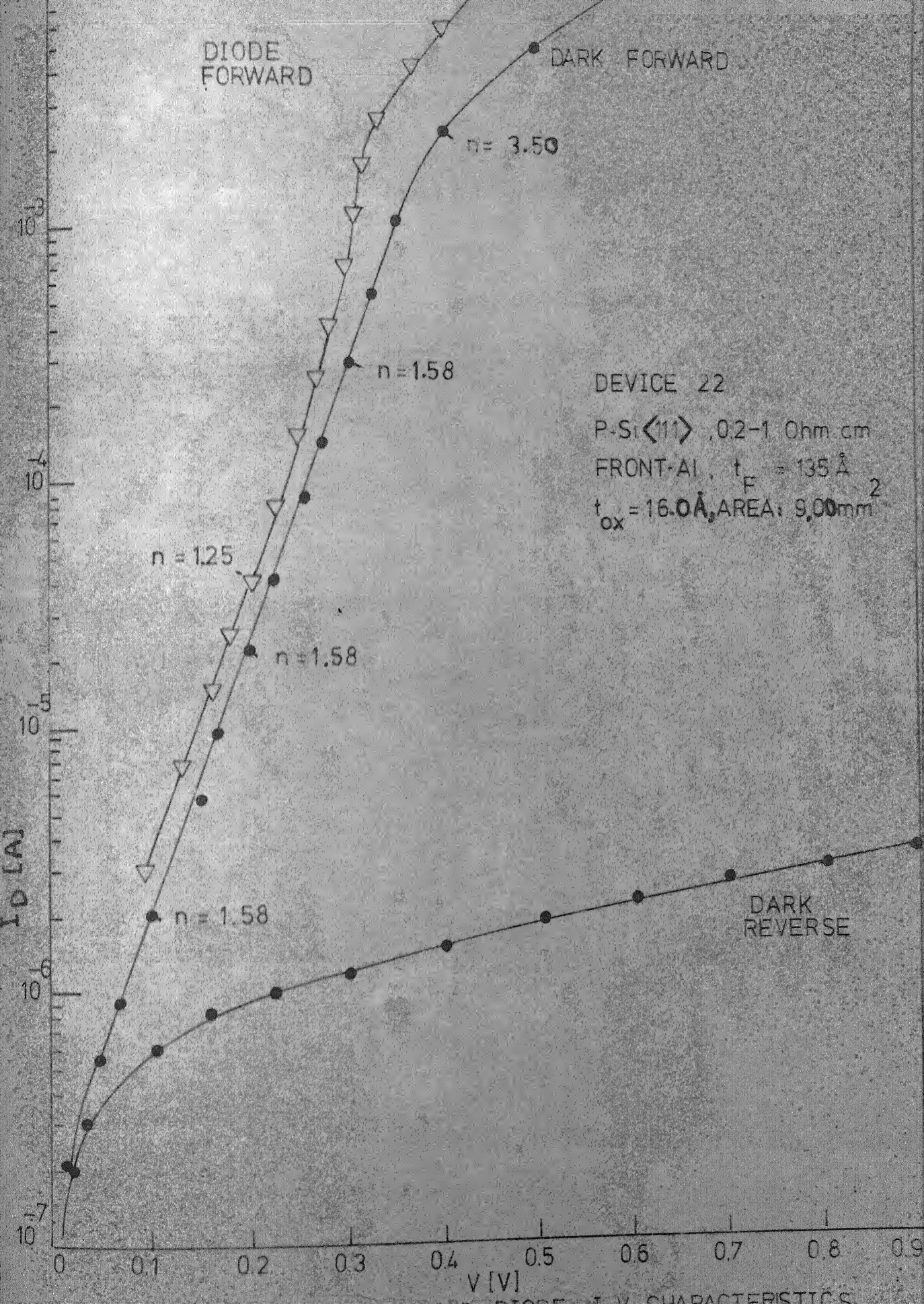


FIG 4.1 DARK AND ILLUMINATED DIODE I-V CHARACTERISTICS


DIODE
FORWARD
DARK FORWARD
n= 3.50
n=1.58
DEVICE 22
P-Si ⟨11⟩ ,0.2-1 Ohm cm
FRONT-Al , t_F = 135 Å
t_{ox} = 16.0Å, AREA: 9,00mm^2
n = 1.25
n=1.58
n = 1.58
DARK
REVERSE
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
ID [A]
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
V [V]

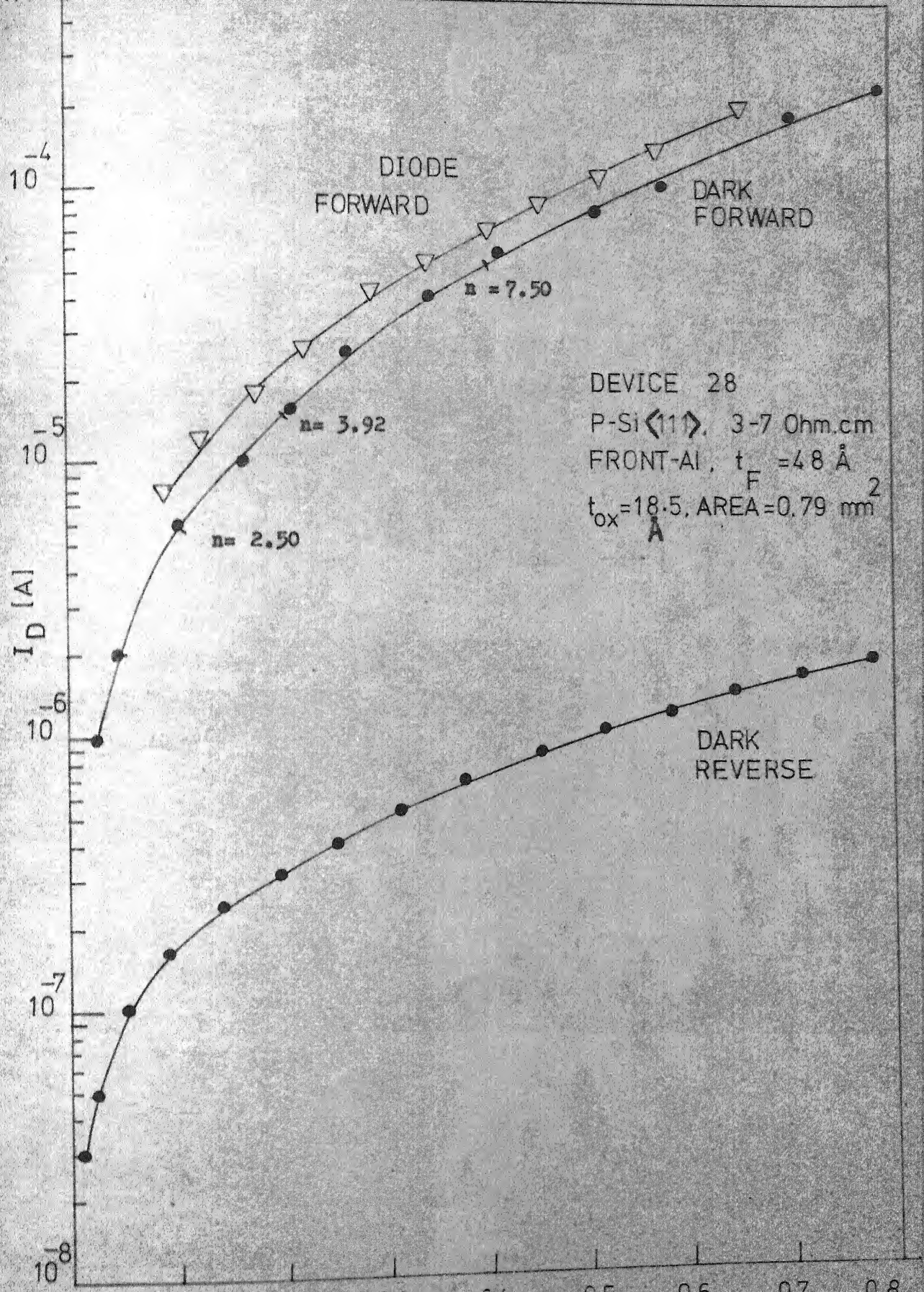
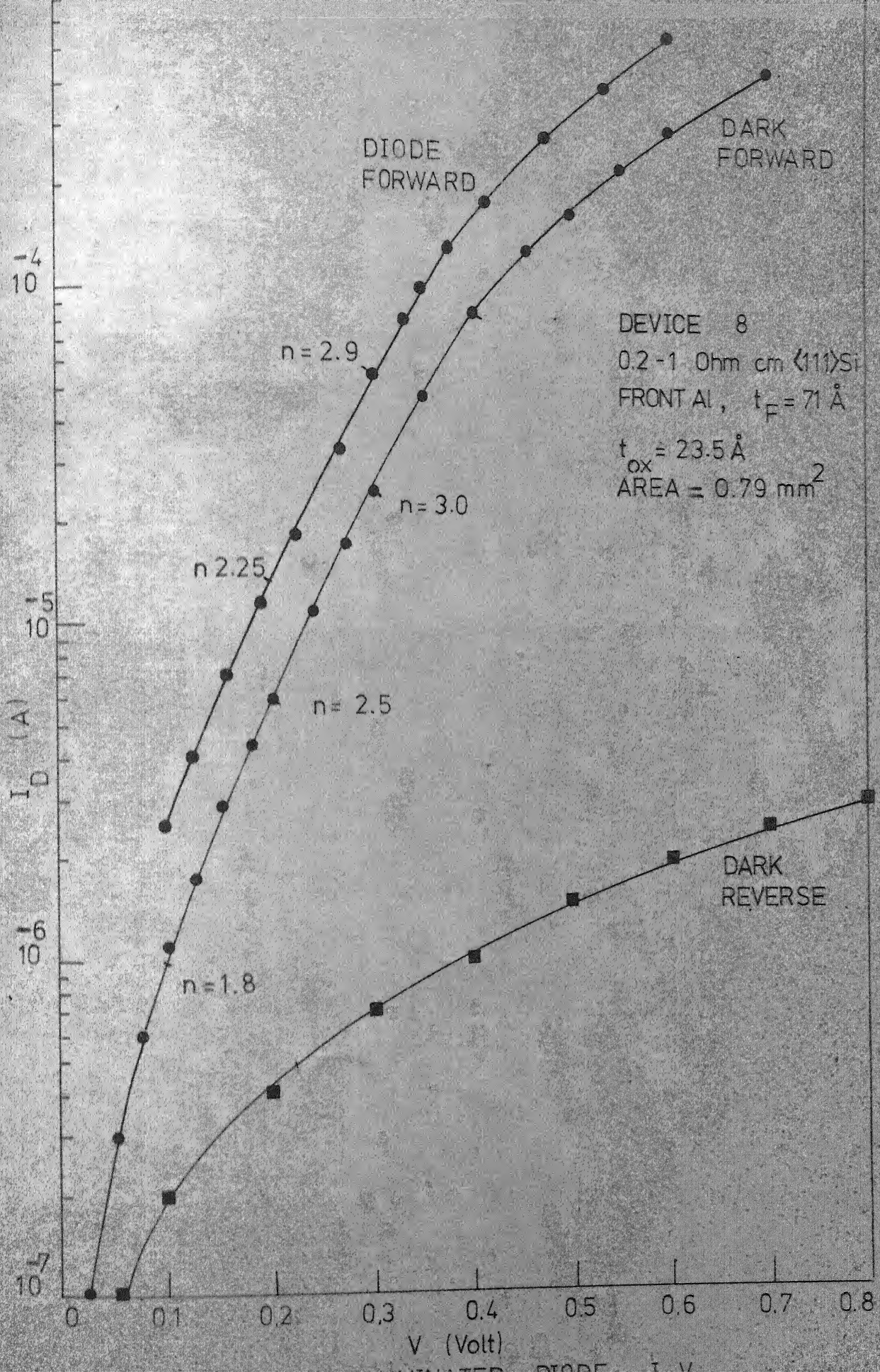
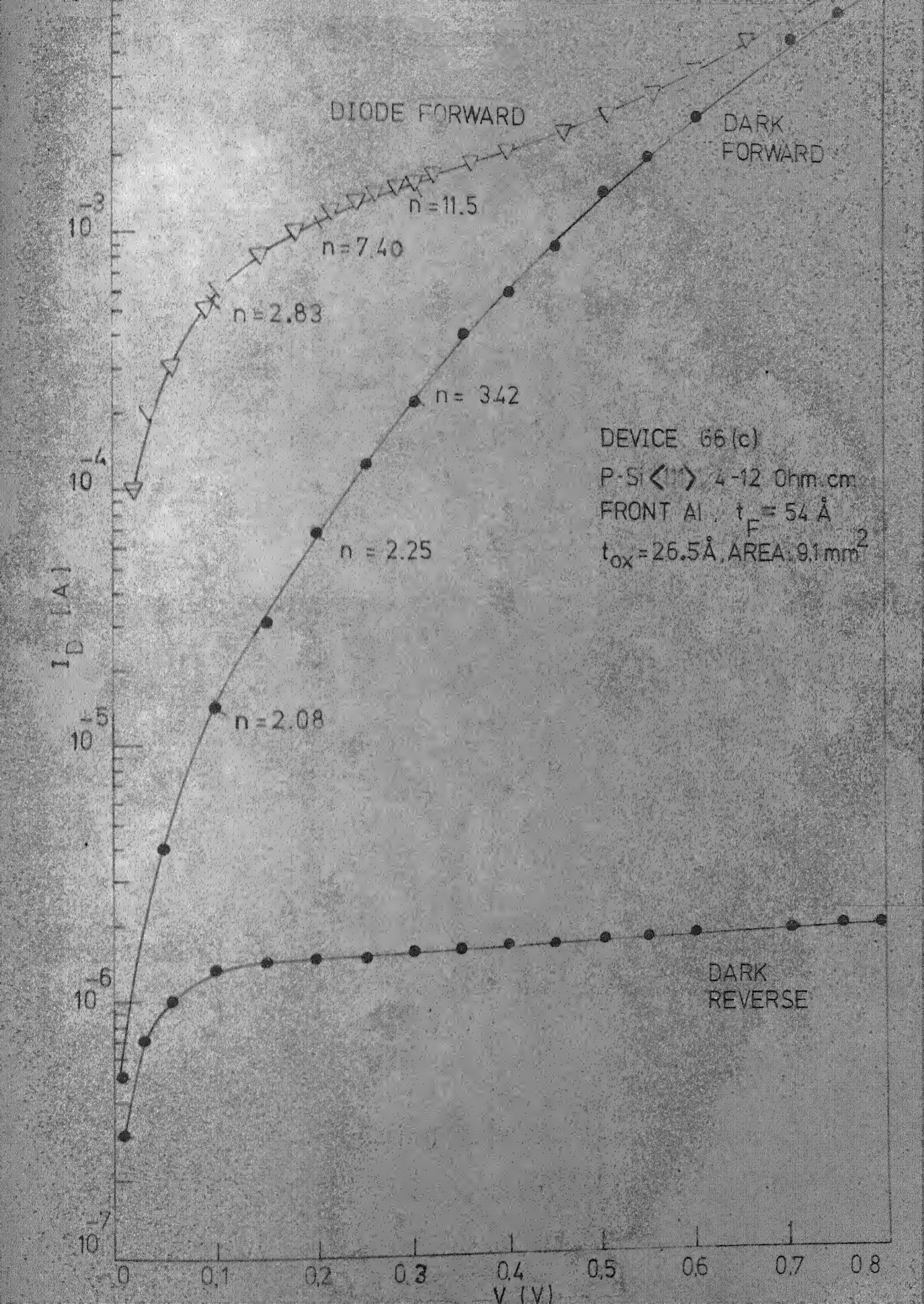


FIG.4.3 DARK AND ILLUMINATED I-V CHARACTERISTICS OF DEVICE 28


DIODE
FORWARD
DARK
FORWARD
DEVICE 8
0.2 - 1 Ohm cm ⟨111⟩Si
FRONT Al, t_F = 71 Å
t_{ox} = 23.5 Å
AREA = 0.79 mm^2
n = 2.9
n = 3.0
n 2.25
n = 2.5
n = 1.8
DARK
REVERSE
10^{-4}
10^{-5}
10^{-6}
10^{-7}
I_D (A)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
V (Volt)


DIODE FORWARD
DARK FORWARD
n = 11.5
n = 7.40
n = 2.83
n = 3.42
n = 2.25
n = 2.08
DEVICE 66 (c)
P-Si <1 1 1> 4-12 Ohm cm
FRONT Al , t_F = 54 Å
t_{ox} = 26.5Å, AREA: 9.1 mm^2
DARK REVERSE
I_D [A]
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
V (V)

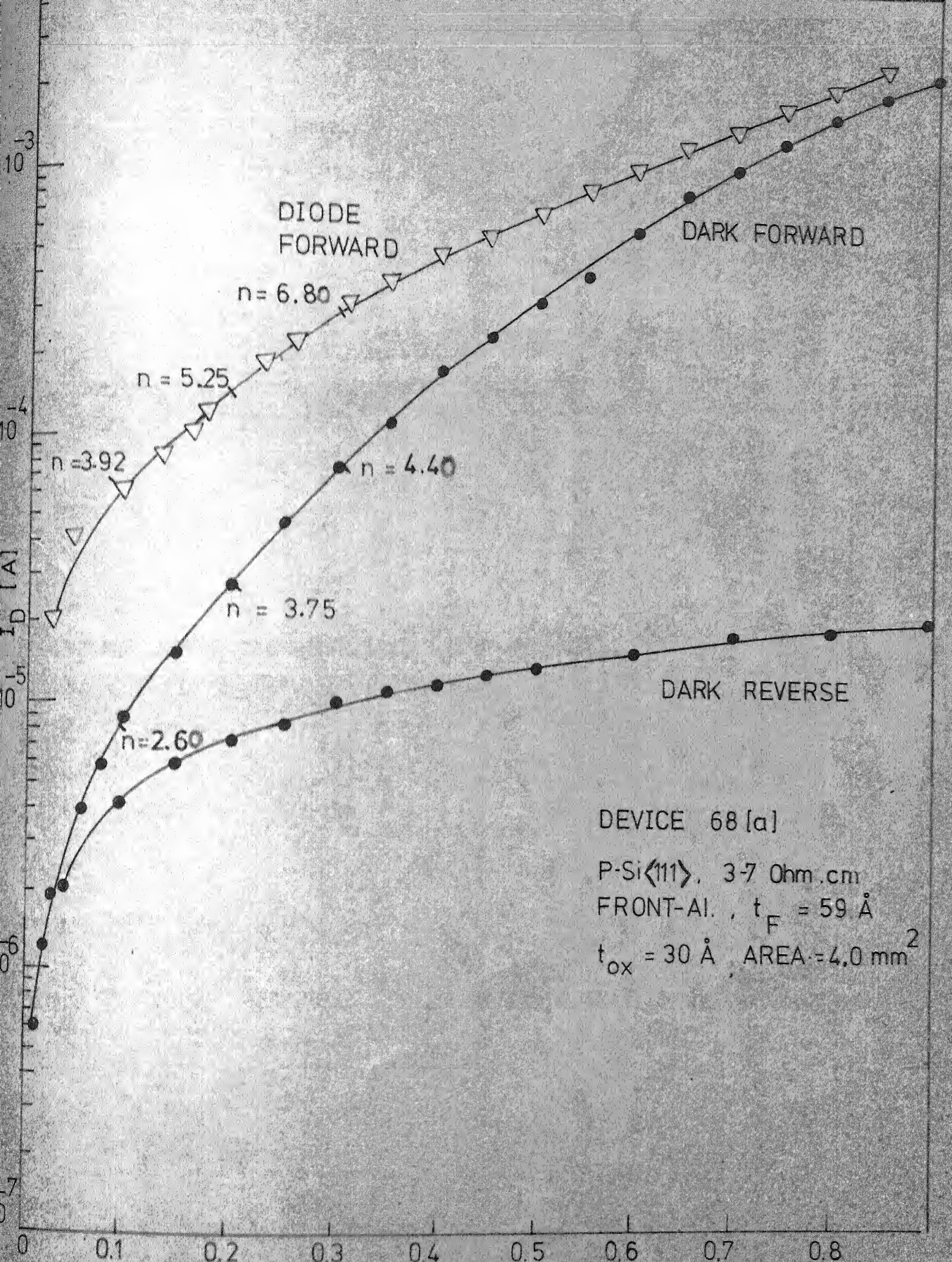
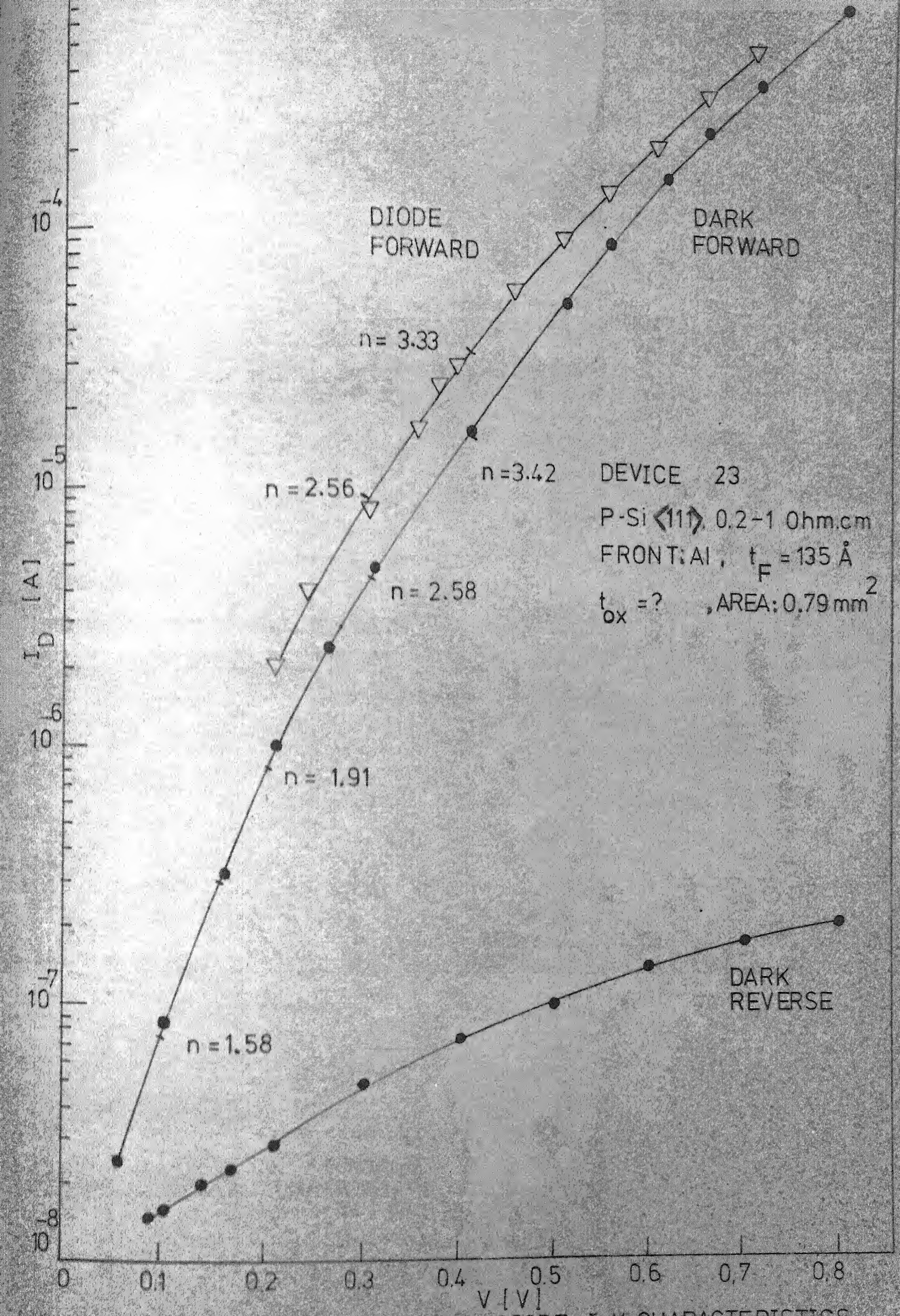


FIG.4.6 DARK AND ILLUMINATED DIODE I-V CHARACTERISTICS OF DEVICE 68 [a]


DIODE
FORWARD
DARK
FORWARD
n= 3.33
n =3.42
n = 2.56
n = 2.58
n = 1.91
n = 1.58
DARK
REVERSE
DEVICE 23
P-Si ⟨111⟩, 0.2-1 Ohm.cm
FRONT: Al , t_F = 135 Å
t_{ox} = ? , AREA: 0.79 mm^2
I_D [A]
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
V [V]

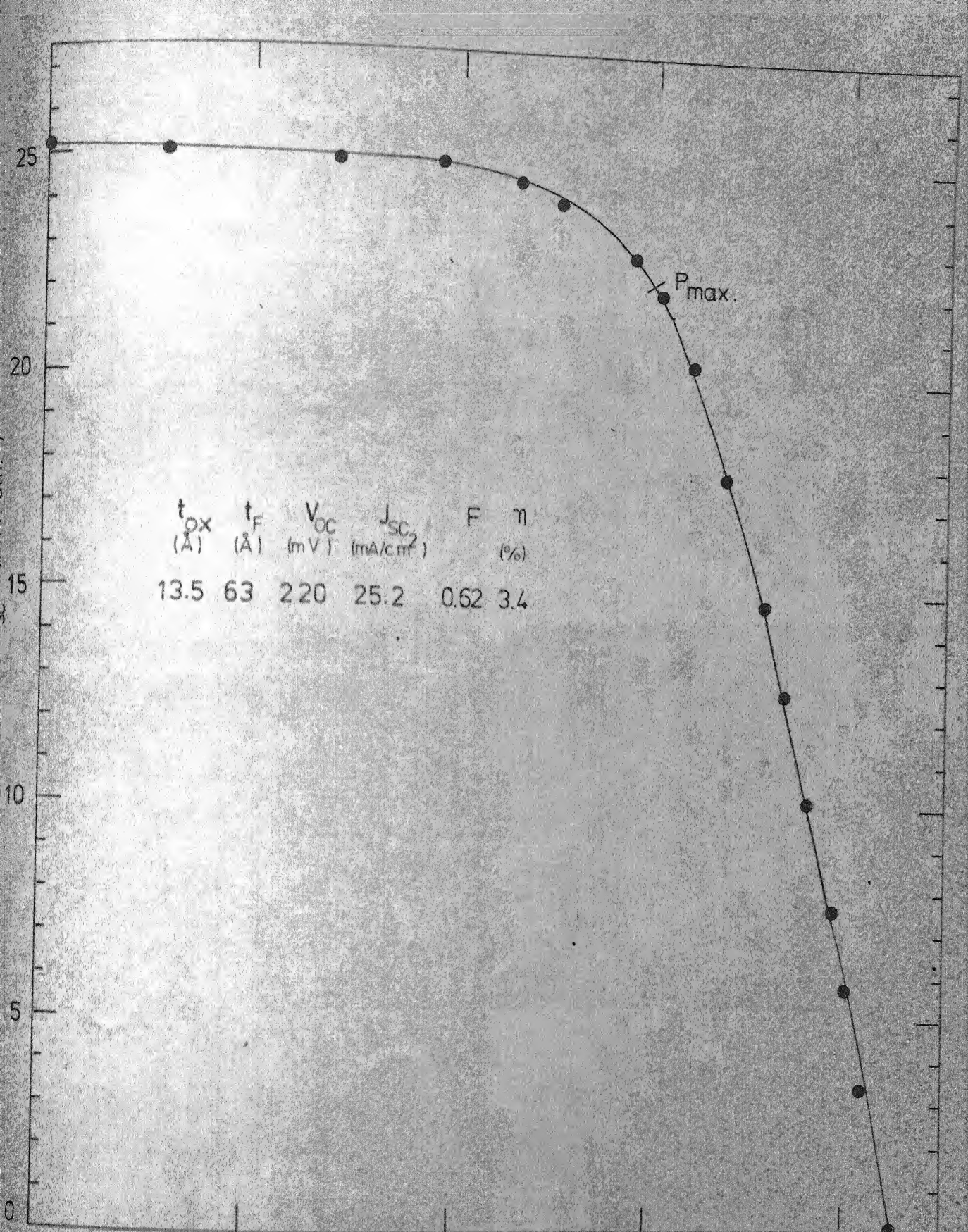


FIG.4.8 SOLAR I-V CHARACTERISTICS OF DEVICE No.74

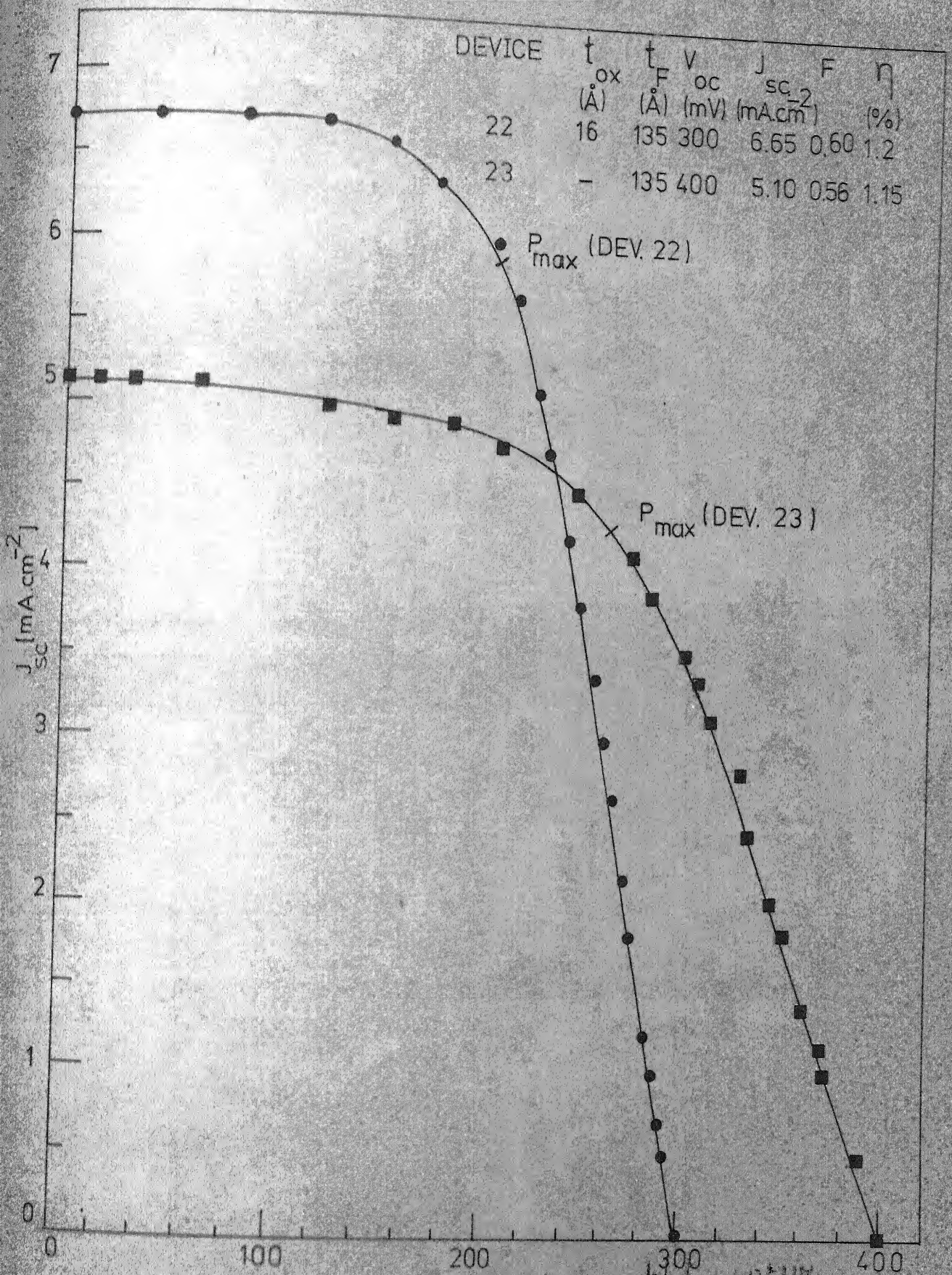


FIG.4.9. SOLAR I-V CHARACTERISTICS OF DEVICES 22 AND 23

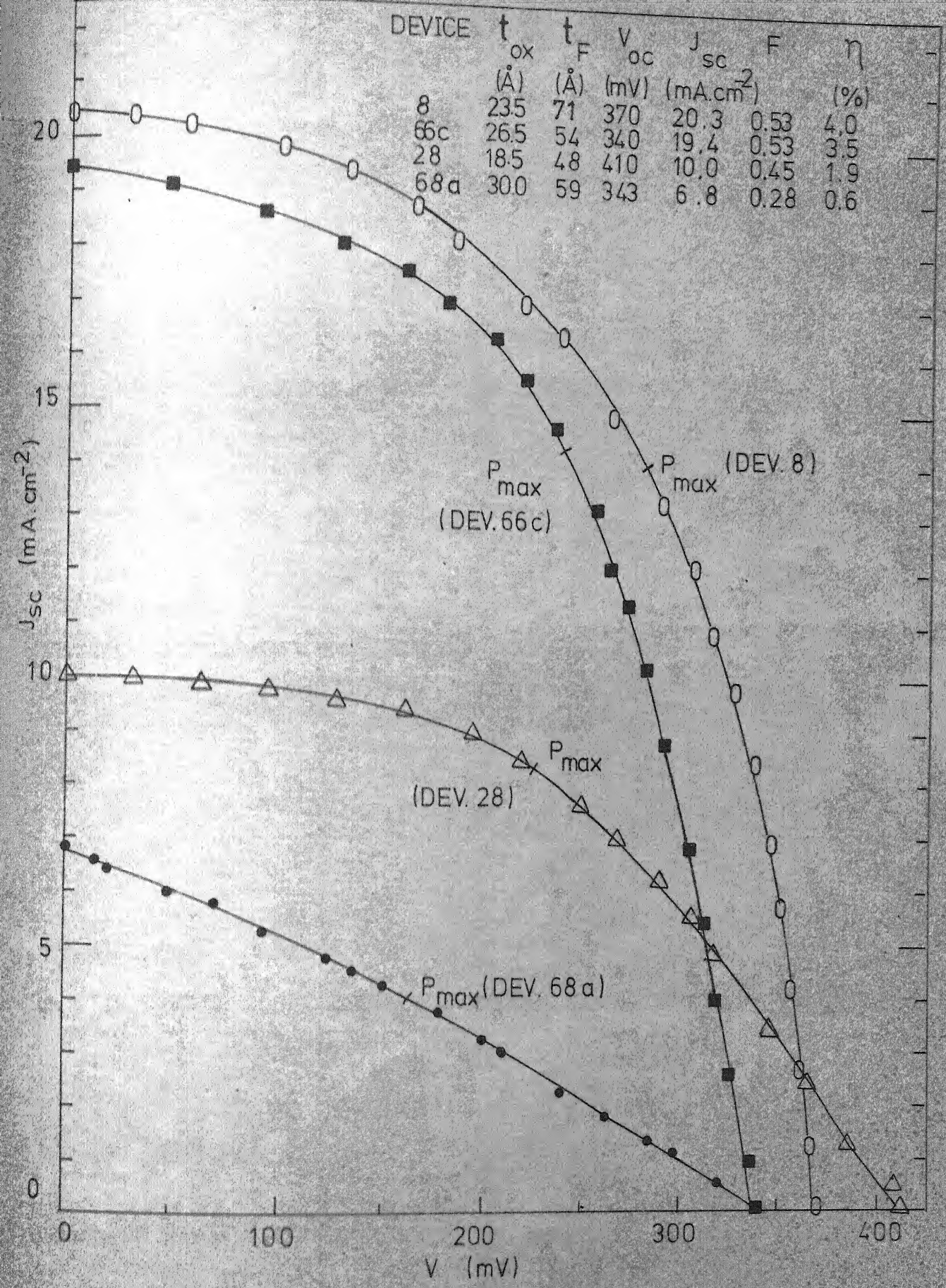


FIG. 4.10 SOLAR I-V CHARACTERISTICS OF DEVICES 8, 66C, 28, 68(a)

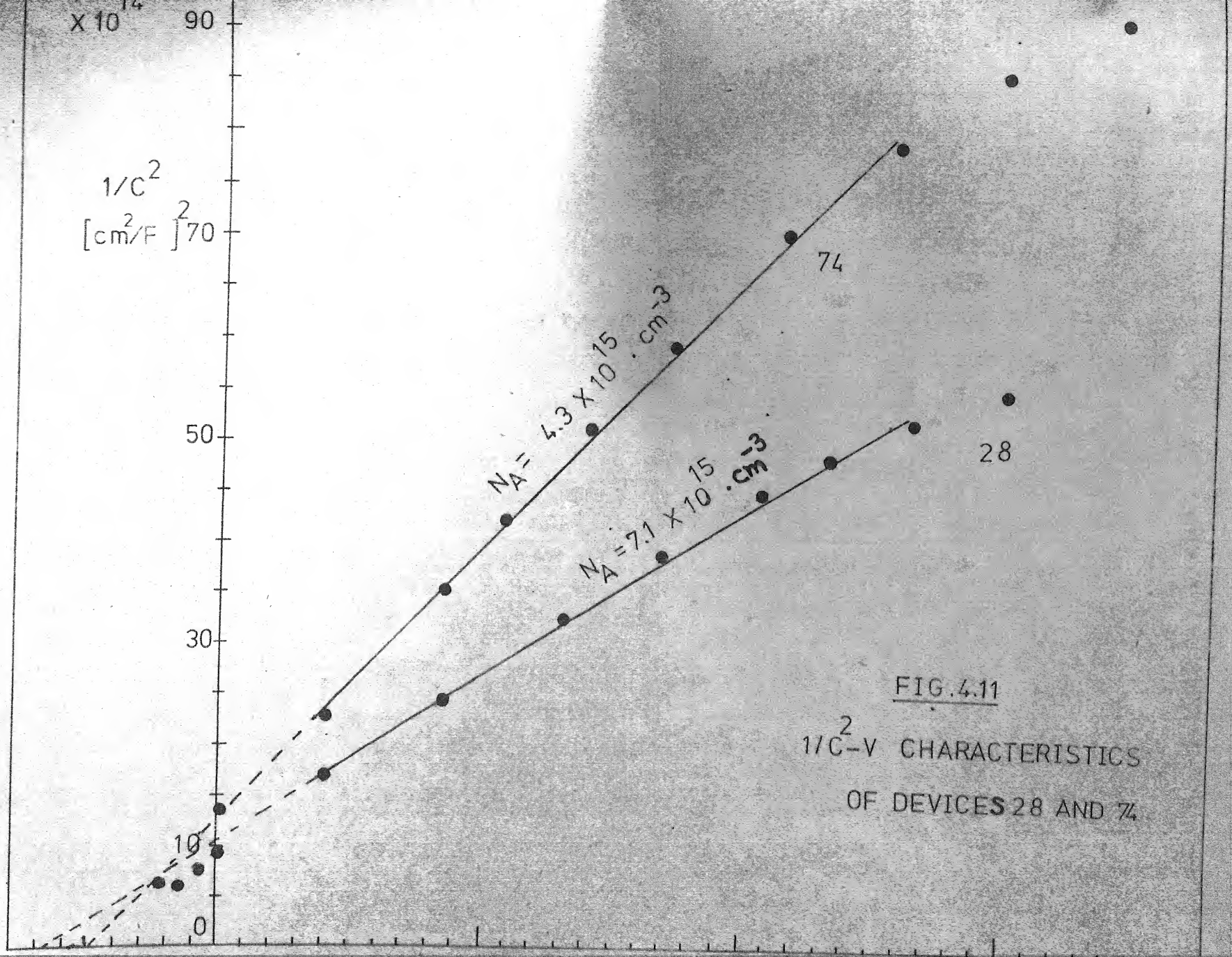


FIG. 4.11

$1/C^2$-V CHARACTERISTICS OF DEVICES 28 AND 74

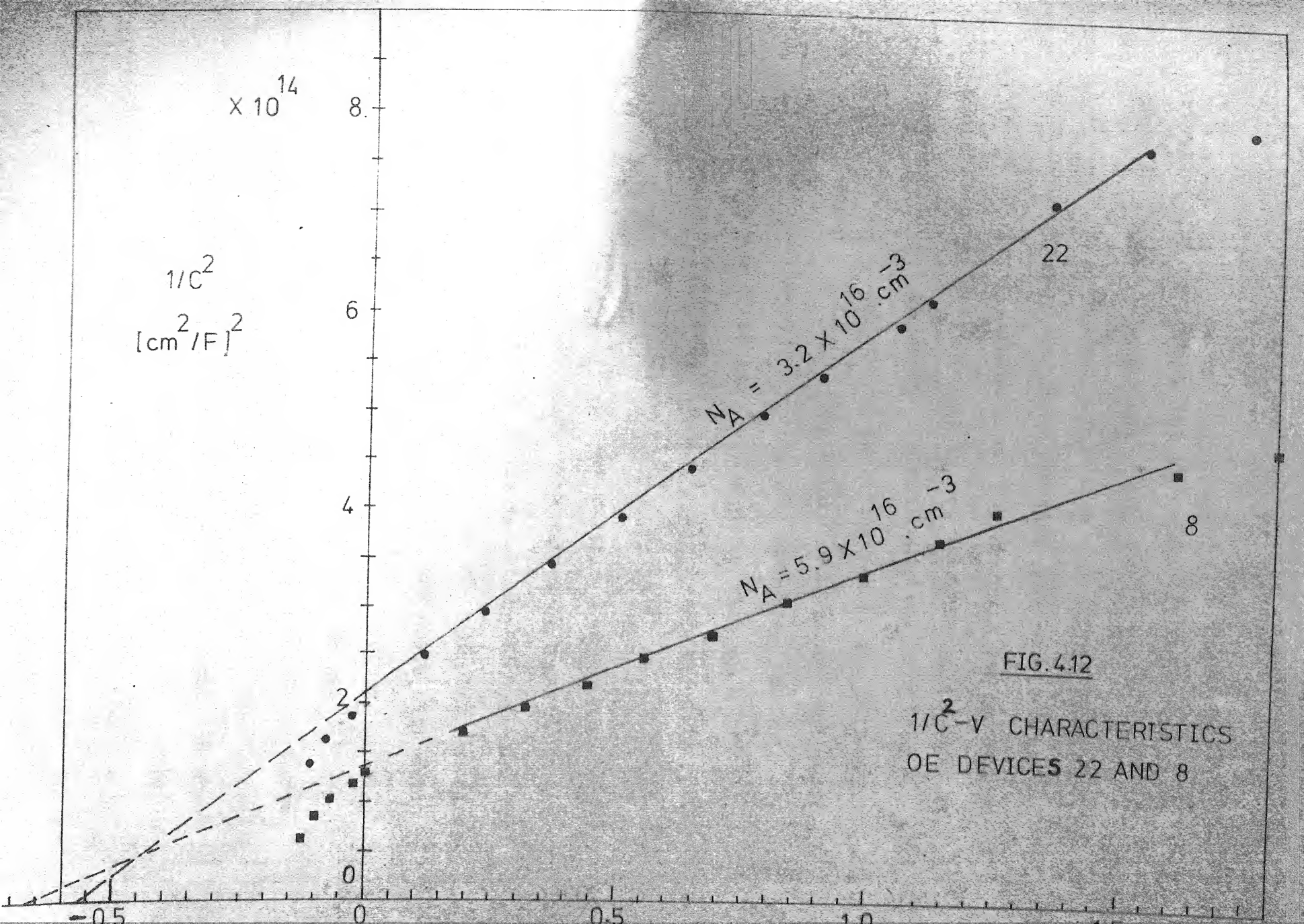


FIG. 4.12

$1/C^2$-V CHARACTERISTICS OE DEVICES 22 AND 8

it difficult to measure the average oxide thickness less than 20 Å from this method.

Therefore, oxide thickness of the present devices have been estimated from the earlier data obtained by Archer[31] from ellipsometry. The error in the estimation of the average oxide thickness is not more than ± 2 Å. It is worthwhile mentioning that for current, the effective oxide thickness is determined by the thickness of the thinnest region and not by the average oxide thickness. The current is so sensitive to non-uniformity in the oxide thickness because tunneling has a steep exponential dependence on t_{ox}.

DARK I-V CHARACTERISTICS

The log I-V characteristics of aluminium devices are shown in Figures 4.1-4.7. The values of 'n' at different biases are also included in Table 4.3. The SBSC (Device 74) shows an almost linear log I-V plot (n = 1.04) when the diode is forward biased in dark. Similarly, MOS cells with oxide thickness upto 16.0 Å show an almost linear forward characteristics. The large scale departure of the current from an exponential form for thicker oxides is due a number of factor[32]. One of them is the dependence of the tunneling probability on the bias. A second important factor is the effect of the voltage drop across the oxide on the change in

silicon band-bending. The second factor becomes more pronounced with increasing oxide thickness and causes the log I-V characteristic to droop. The third factor is excess current arising out of interface recombination. All the above three factors make n strongly dependent on voltage, as Figures 4.3-4.7 and Table 4.3 vividly illustrate. These also show that the value of n generally increases with oxide thickness.

ILLUMINATED DIODE I-V CHARACTERISTICS

It has been predicted theoretically[30] that the behavior of interfacial layer is quite different under illumination than that in the dark. Under illumination, the surface states communicate readily with the minority carriers whereas in dark they communicate with the majority carriers. On the basis of their theoretical analysis, Card and Yang[30] predicted n to approach 1.0 under illumination in case of MOS solar cells.

This prediction is not borne out by our experimental results. In fact Figs.4.1-4.7 and Table 4.3 show just the opposite to happen. The I-V measurements indicate that under illumination the diode current increases and so does in general the value of n. The increase in diode current may be due to enhanced bulk recombination, however, from the

fact that the increase in diode current becomes more pronounced for thicker oxides, one may conclude that the increase in diode current is mainly due to a reduction in silicon band-bending under light. Under light, for p-type silicon, the interface charge becomes more negative, because the electron quasi-Fermi level controls the occupancy of interface states. This causes a higher oxide voltage and lower silicon band-bending. These conclusions are just the reverse of what Card and Yang made without the benefit of experimental evidence on I-V characteristics. The open-circuit voltage in all the cases, i.e. Figures 4.1-4.7 corresponds to a diode current $I_D = I_L$ which is closer in value to the one given by the illuminated I_D-V characteristics rather than by the dark I-V characteristics.

DOPING CONCENTRATION

The doping concentration (N_A) can be determined from the slope of $1/C^2$-V characteristics. The plots of $1/C^2$-V for devices 74, 28, 22 and 8 are included in Figures 4.11 and 4.12. The observed acceptor impurity concentration shows a close agreement with the corresponding values obtained from resistivity data, cf. Table 4.4.

BARRIER HEIGHT

Table 4.4 presents the barrier height data obtained from $1/C^2$-V characteristics under dark. The barrier height was calculated by adding ϕ_p and kT/q to the voltage axis intercept V_i. Considering the inaccuracies in different measured parameters it can still be concluded that the results indicate the barrier height to increase with the oxide thickness. This has been observed by other investigators[8,22,16] in case of MOS devices with Al contact on p-type silicon. Therefore the increase in V_{oc} can at least partially be attributed to the increased barrier height. However, it should be kept in mind that the increase in barrier height is likely to be lower under illumination.

OPTIMUM THICKNESS OF ALUMINIUM FILMS AND J_{sc}

In order to obtain the optimum thickness of aluminium films, we started with a very simple consideration i.e. the transmittance to sheet resistance ratio ($T(\lambda)/R_{\square}$) should be maximum at the optimum thickness of the film. On the ground of this assumption, optimum film thickness was estimated by plotting $T(\lambda)/R_{\square}$ as a function of aluminium film thickness, cf. Figure 4.13. $T(\lambda)$ and $R_{\square}$ data for this purpose were taken from the results obtained

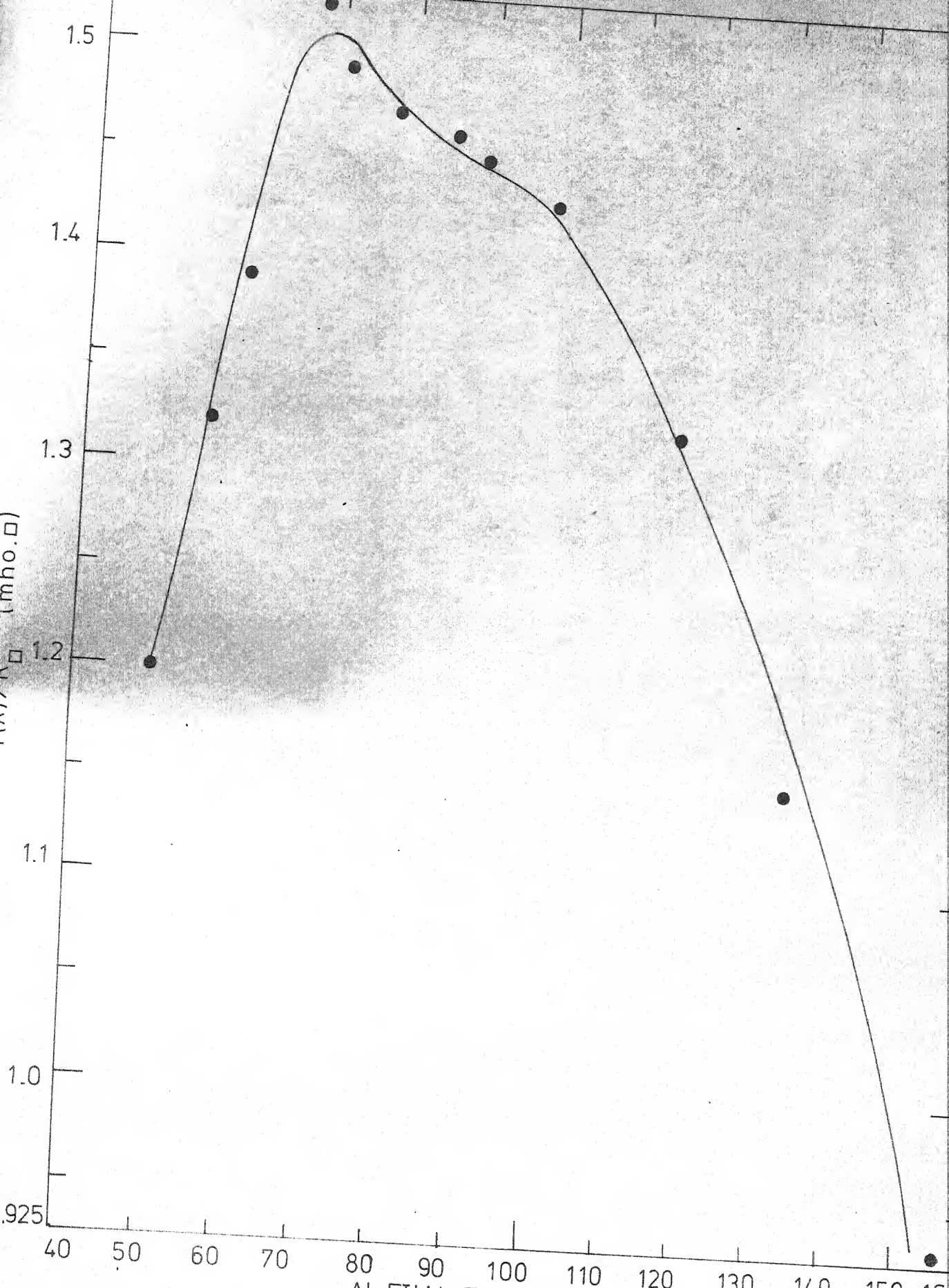


FIG. 4.13 . VARIATION OF T(λ)/R WITH

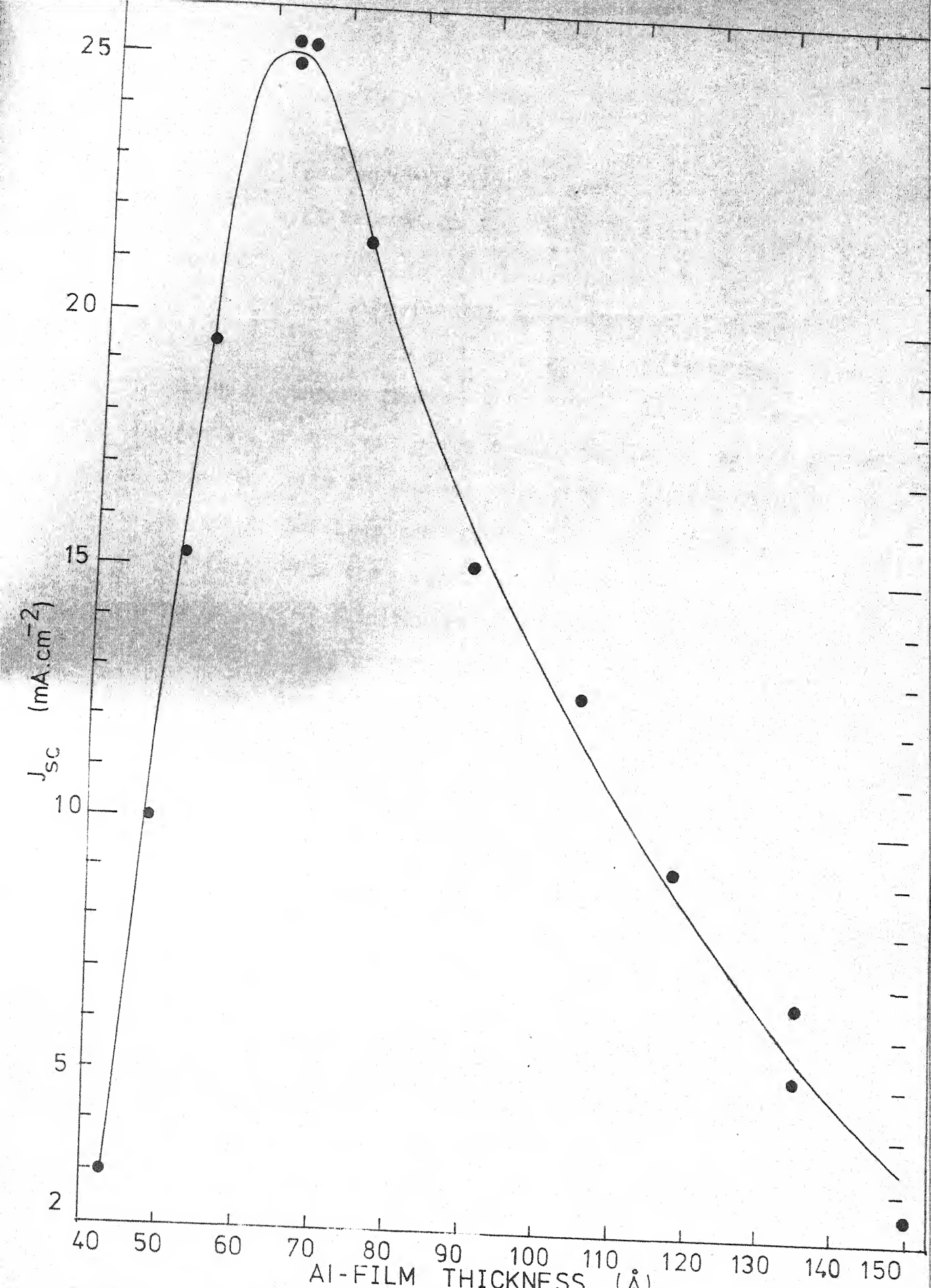


FIG.4.14. EFFECT OF Al-FILM THICKNESS

by Bond[19] (see Appendix II). Figure 4.13 suggests that $T(\lambda)/R_{\square}$ will be maximum for about 70 Å thick aluminium films.

For the experimental determination of optimum film thickness, aluminium SBSC's were fabricated with film thicknesses ranging from 45 Å to 150 Å. Figure 4.14 shows the variation of short circuit current density as a function of aluminium film thickness. The curve, cf. Figure 4.14, which was fitted into the experimental data with the help of IBM 7044 using the method of least squares, shows a maxima around 63 Å thickness of Al film. The drop in J_{sc}, for film thickness greater than 63 Å, can be attributed to the sharp decay of $T(\lambda)$ with increasing film thickness, whereas, for film thicknesses smaller than 63 Å the reduction in J_{sc} can be due to discontinuity in the films and due to increase in the sheet resistance of the films.

It is quite encouraging to note that the experimental observations are in close agreement with the theoretically predicted value of the optimum film thickness.

Figure 4.14 can be useful for investigating the effect of oxide thickness on J_{sc}. Fot plotting the curve, it has been assumed that in an SBSC ($t_{ox} \approx 10$ Å) the oxide is completely transparent to the flow of light generated minority carriers and hence does not affect the J_{sc}. However,

in MOS solar cells with thick oxides, J_{sc} may get reduced. For an MOS solar cell, with known Al film thickness, the observed J_{sc} can be compared with the expected value of J_{sc} of an SBSC having the same Al-film thickness. By doing that, any difference observed in two J_{sc}'s can be attributed to the change in transport properties of the oxide layer.

It has been observed that upto a thickness of 18.5 Å, the oxide does not affect the J_{sc}, whereas, with oxides thicker than 23.5 Å a reduction in J_{sc} takes place. For example, on the basis of Al-film thickness considerations only, device 68(a) is expected to give a J_{sc} = 24.5 mA/cm^2, whereas, the observed value of J_{sc} is only 6.8 mA/cm^2, cf. Table 4.2. From this fact and the effect of oxide thickness on the open-circuit voltage as illustrated by Table 4.2, it may be said that the optimum oxide thickness lies in the range of 19 to 24 Å.

SERIES RESISTANCE AND FILL FACTOR

To see the effect of series resistance on the performance of an SBSC, Device 74 was connected to Tektronix (Type 575) curve tracer in series with a decade resistance box. Figure 4.15 shows AM1 solar I-V characteristics of the cell as a function of series resistance.

Since, we have fabricated cells with different areas, to make the comparative assessment easier, we have multiplied

the series resistance of each cell by its area. This gives the equivalent series resistance R_s' in Ohm.cm^2. The series resistance was computed from the forward I-V characteristics of the devices at large biasing voltages.

Figure 4.15 shows that a series resistance of 200 Ohms (R_s' = 6.28 Ohm.cm^2) can reduce the fill factor from 0.62 to 0.50, whereas R_s of 1 K Ohm (R_s' = 31.4 Ohm.cm^2) will not only bring down the fill factor to 0.16 but will also reduce the short circuit current density from 25.2 mA/cm^2 to 15.2 mA/cm^2. R_s and R_s' for various cells are included in Table 4.2.

The highest fill factor achieved is 0.62, which is comparable to the results obtained by earlier investigators on p-type silicon SB/MOS cells. It can be seen that in the case of device 68(a) ($t_{ox} \sim 30$ Å, R_s = 1.2 K Ohm, R_s' = 48 Ohm.cm^2 the fill factor is only 0.28.

EFFECT OF INPUT POWER ON V_{oc} & I_{sc} OF Al-MOS SOLAR CELL

Figure 4.16 shows the effect of input power level on V_{oc} and I_{sc} of Al-MOS solar cell (Device 25). P_{in} for this purpose was adjusted with the help of OCLI p-n junction solar cell (see Appendix IV).

I_{sc} was found to increase linearly with P_{in}, whereas, V_{oc} first increases rapidly and then becomes less dependent on input power. These observations agree with the earlier observations by Charlson and Lien[8].

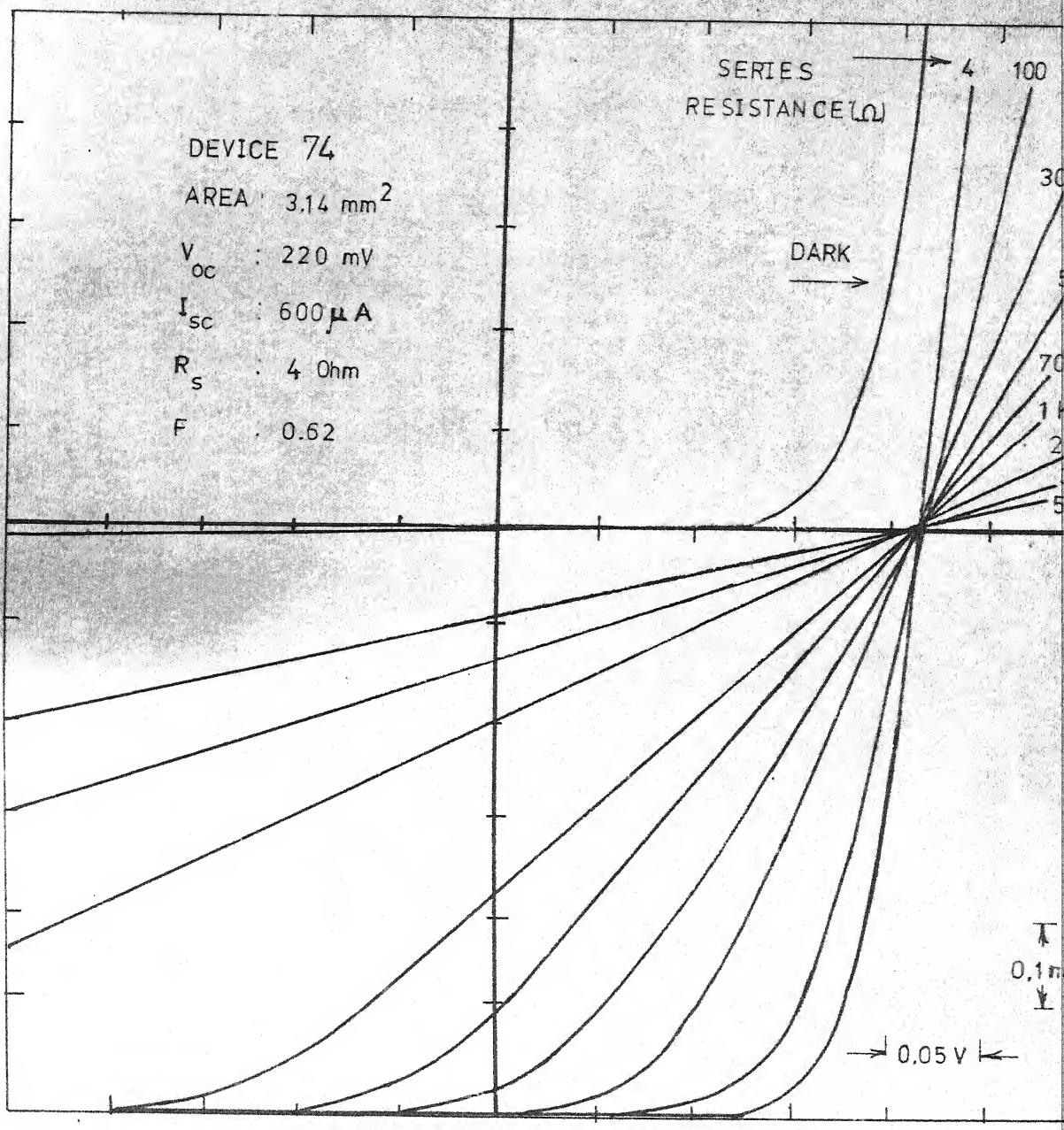
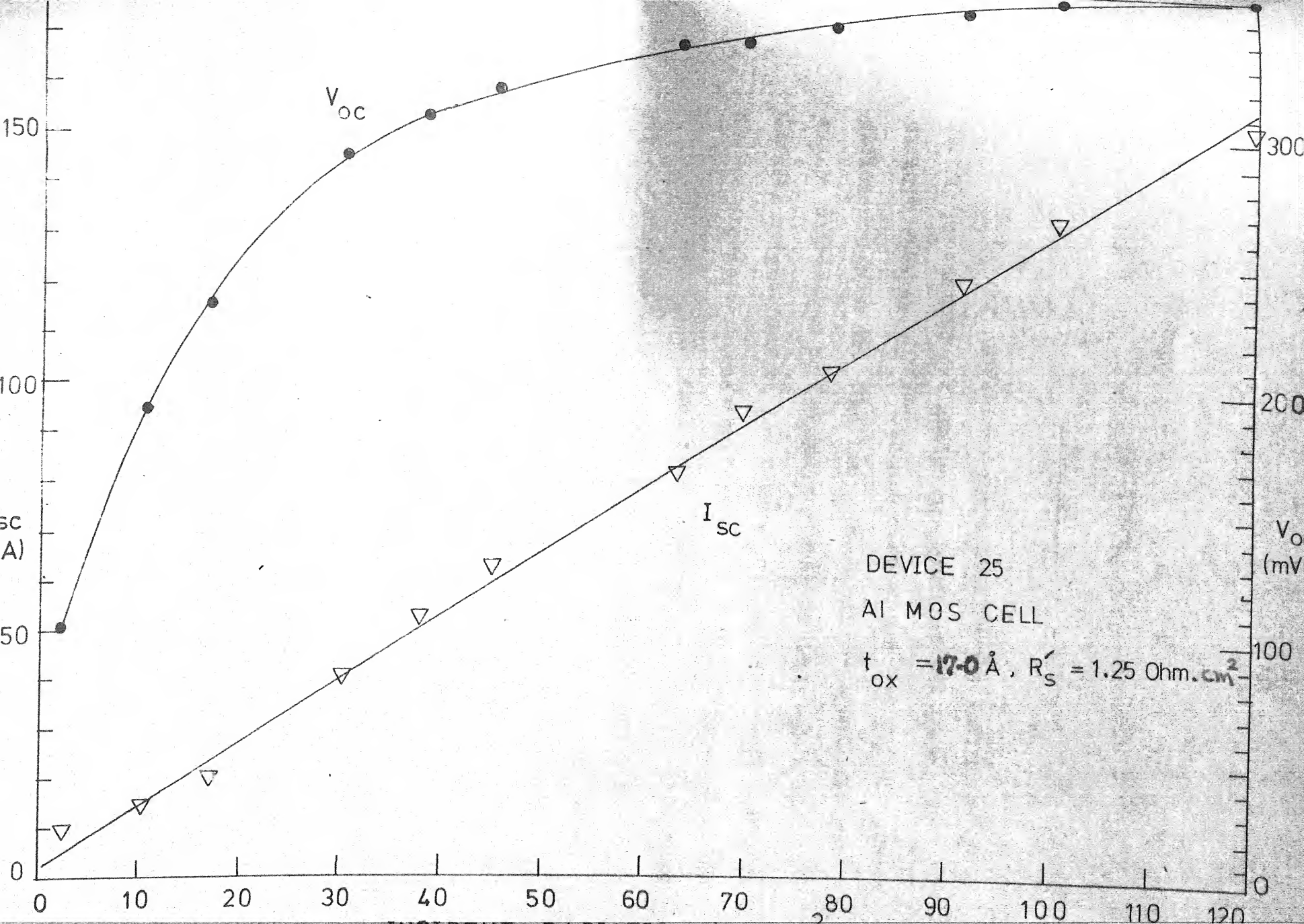


FIG. 4.15 . EFFECT OF SERIES RESISTANCE ON THE PERFORMANCE OF AN S B S C .


V_{oc}
I_{sc}
DEVICE 25
Al MOS CELL
t_{ox} = 17.0 Å, R_s' = 1.25 Ohm.cm²
150
100
50
0
300
200
100
0
0
10
20
30
40
50
60
70
80
90
100
110
120

CHAPTER V

CONCLUSIONS

Cr and Sn devices fabricated in the initial stage of the present investigation have indicated poorer open circuit voltage, short circuit current and overall conversion efficiency than Al. The low open circuit voltages observed can be attributed to low barrier heights achieved. The barrier heights may be low because of possible contamination due to excessive degassing during the evaporation of these metals or due to the fact that metal atoms can penetrate into silicon surface when evaporations are conducted at high temperatures. This would create interface states and bring down the barrier height. Moreover, Cr and Sn films have been observed to degrade rapidly when exposed to air, resulting in rapid degradation of device performance.

Present investigation has indicated that high conversion efficiencies can be achieved for Al-SB/MOS solar cells with antireflection coating. In the case of Al-SBSC's an open circuit voltage in the range of 200-220 mV can be achieved. With increase in the interfacial oxide thickness, zero bias band bending has been observed to increase. This observation is in agreement with the earlier observations[8,22]. However, open circuit voltage has been found to increase

with increasing oxide thickness only upto 19 Å, a maximum V_{oc} = 410 mV has been observed at this thickness of interfacial layer.

With further increase in oxide thickness both V_{oc} and J_{sc} have been observed to decrease. The optimum oxide thickness seems to lie in the 19-24 Å range. Devices, with oxide thickness near 30 Å, show an extremely high series resistance and poor fill factor. The highest open-circuit voltage achieved by us without antireflection coating, is 410 mV, highest short-circuit current density 25.2 mA/cm^2, highest fill factor 0.62, and the highest efficiency 4.05 percent. The highest values reported in the literature[8] for these parameters are: V_{oc} = 430 mV, J_{sc} = 26.5 mA/cm^2, and η = 8 percent, all with antireflection coating. Since aluminium film has a very high reflectance, a much higher value of J_{sc} and efficiency can be expected with antireflection coating.

The optimum thickness of Al-film has been observed to be about 63 Å, which agrees reasonably well with the theoretical value of optimum Al film thickness predicted by us.

Amongst Al, Au, Ag, Cu and In, gold is found to give the best ohmic contact on p-silicon.

The zero-bias barrier height was found to increase with the oxide thickness in agreement with earlier investigations. However, this may only partially explain the increase in open-circuit voltage. A part of the reason for increase in V_{oc} has to lie in the fact that the oxide reduces the diode current but does not affect the light-generated minority carrier current so long as the oxide thickness does not exceed a certain critical value. This is so because any barrier presented by the oxide will reduce the majority carrier diode current. However, the minority carrier light-generated current is affected only when the minority carrier tunneling time becomes less than the diffusion time of minority carriers throu silicon.

The diode quality factor n was found to increase with oxide thickness and in general also with light intensity. Also, the diode current was higher under illumination than in dark. This indicates that under light the interface state occupancy is given by the minority carrier quasi-Fermi level leading to a more negative charge for p-type silicon. Consequently the oxide voltage increases, the silicon band-bending decreases giving rise to an increase diode current. These findings are just the reverse of what was predicted by Card and Yang[30] on the basis of theoretical analysis.

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APPENDIX - I

NATURAL OXIDE GROWTH ON SILICON

The thickness and growth kinetics of oxide films on polished silicon, exposed to room air after having been rinsed in hydrofluoric acid, have been studied by Archer[31].

The ellipsometeric measurements show that immediately after HF rinse the films are 10-15 Å thick and increase in thickness by about 11-12 Å after one day in air.

The film growth data accord reasonably well with the Elovich equation,

$$L = a + b \log(t + t_o) \qquad \text{(i)}$$

where L is the oxide thickness, t is the time and a,b and t_o are constants.

For silicon, equation (i) becomes

$$\underset{(\text{Å})}{L} = -9.74 + 6.86 \log \underset{(\text{sec.})}{(t + 1500)} \qquad \text{(ii)}$$

Equation (ii) can be represented in the graphical form as shown in Figure A1. The uncertainty in the calculation of thickness is $\pm$ 2 Å.

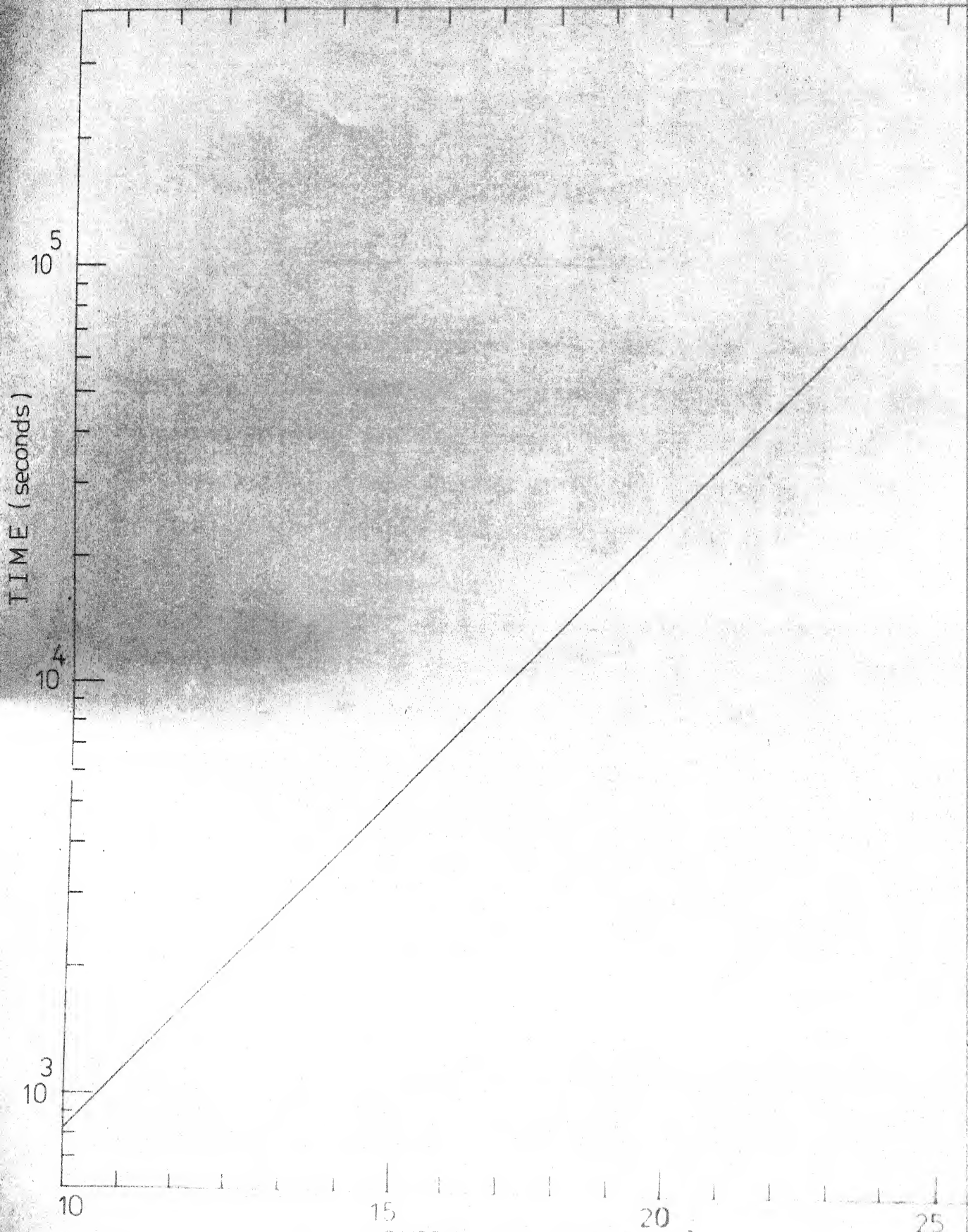

FIG. A1 : OXIDATION CHARACTERISTICS OF SILICON IN
AT 3

APPENDIX - II

STUDY OF THIN ALUMINIUM FILMS

Optical and electrical properties of thin metal films depend on substrate cleanliness, substrate temperature, evaporation rate, residual gases, and vacuum level during the deposition. While this is true for all metals, it is particularly noticeable with oxygen gettering metals like aluminium.

For the purpose of solar cell design, the knowledge of electrical and optical properties of thin metal films is very essential. Unfortunately there is a dearth of relevant data in the literature. Table (a) summarises the available results of investigations on thin aluminium films.

It has been pointed out[18] that high transmittance ($\sim$ 62%) will be obtained for very slow evaporation, where a high percentage of oxygen is present in the film. High oxygen content in the Al film leads to high sheet resistance, for example, non conducting transparent Al-oxide films can be obtained by evaporation of pure Al at 0.5 Å/sec, at an oxygen pressure of 10^{-3} torr. Below 10^{-6} torr pressure, oxygen free conducting metal films, with low transmittances, are obtained.

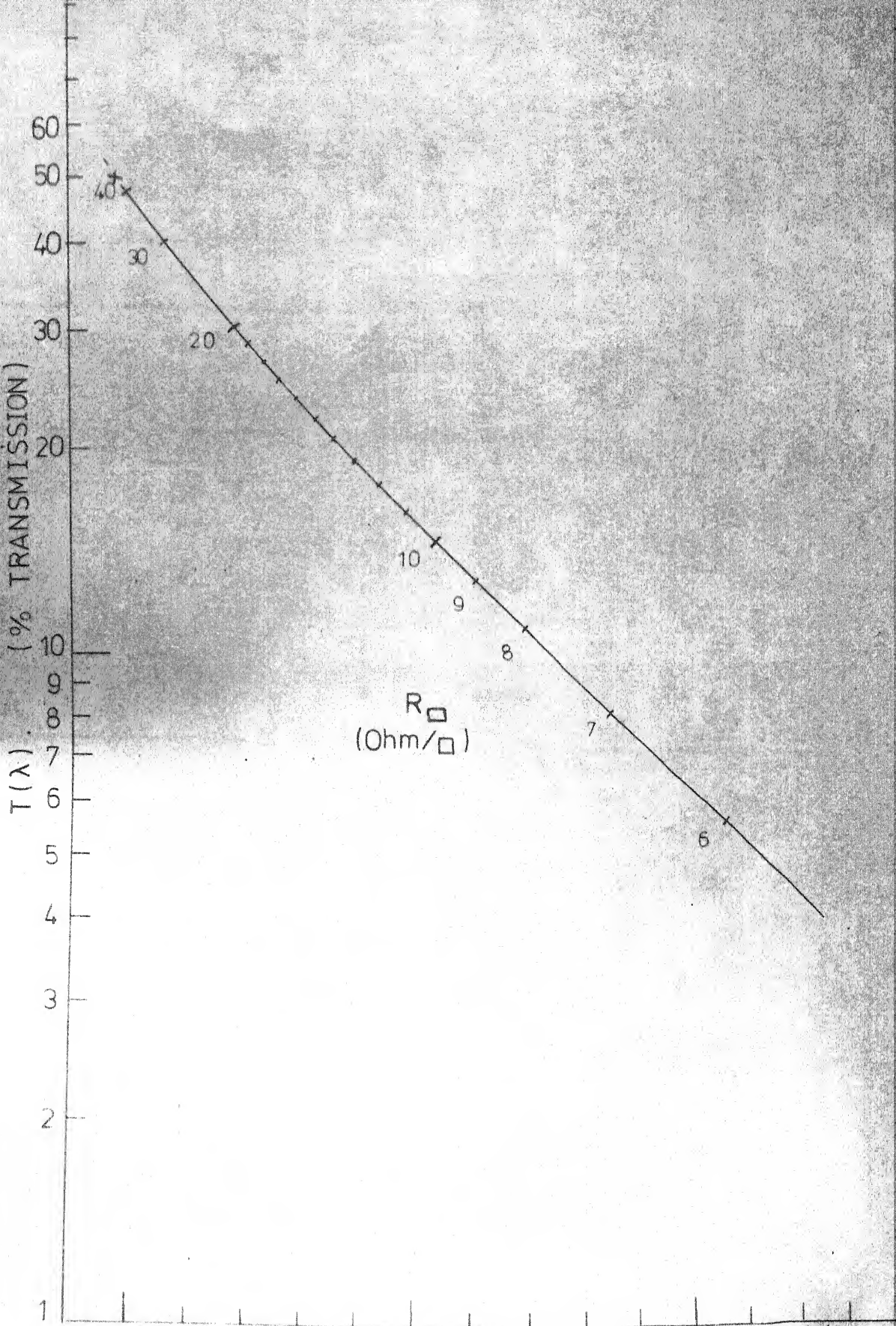

FIG. A2. $T(\lambda)$ and $R_{\square}$ vs THICKNESS OF Al [19]

TABLE (A1)

OPTICAL PROPERTIES OF THIN Al FILMS

SUBSTRATE	FILM THICKNESS (Å)	WAVELENGTH OF LIGHT (Å)	TRANSMI-TTANCE %	REFERENCE
-	75	5000	30	HEAVENS[33]
-	100	5000	18	
GLASS	100	5000	62	CHARLSON[8]
SILICON	75	5000	31	HOVEL[18]
GLASS	75	WHITE	28	BOND[19]
GLASS	100	WHITE	17	

The plot of transmittance and sheet resistance versus aluminium film thickness is given in Figure (A2). The aluminium films were deposited on glass slides at room temperature and at a pressure less than $2X10^{-5}$ torr[19].

APPENDIX - III

CLASS 100 CLEAN SPACE

According to U.S. Federal Standards No. 209(a), 1966 class 100 clean space should meet the following requirements.

(1) It should not have more than 100 particles per cubic foot of size greater than 0.5 micron; no particle should be of size greater than 5 micron and 99.9% of the particle should be of size less than 1 micron.

(2) Temperature: 72°F $\pm$ 5°F (22.2°C $\pm$ 2.8°C)

(3) Humidity : 45%

(4) Laminar air flow rate: 0.45 $\pm$ 0.1 meter per second

(5) Pressure: 0.05" of water higher than the outside pressure.

(6) Lighting: Uniform shadow free 100-150 ft candles intensity.

APPENDIX - IV

OPTICAL MEASUREMENTS

For complete optoelectronic analysis of a solar cell, sophisticated instruments like solar simulator, monochromator, thermopile, radiant flux meter and filter radiometer are generally used. However, in the absence of these instruments meaningful measurements of the significant optical parameters of a test solar cell can be obtained by a relatively simple approach, which uses a calibrated photo diode in conjunction with readily available electronic test equipment.

Silicon photo detectors include p-n junction photocells and photo transistors. Photo cells which have been optimized in design for power generation mode are frequently referred to as solar cells. The current generated by a p-n junction solar cell at any wavelength is proportional to the intensity of the incident radiation and so short circuit current varies linearly with the radiation level.

Figure (A3) shows the short circuit current density as a function of radiation level for OCLI p-n junction solar cell[34].

This solar cell can be used for standardization of the radiation level and for measuring the white light transmittance of thin metallic films, deposited on glass slide.

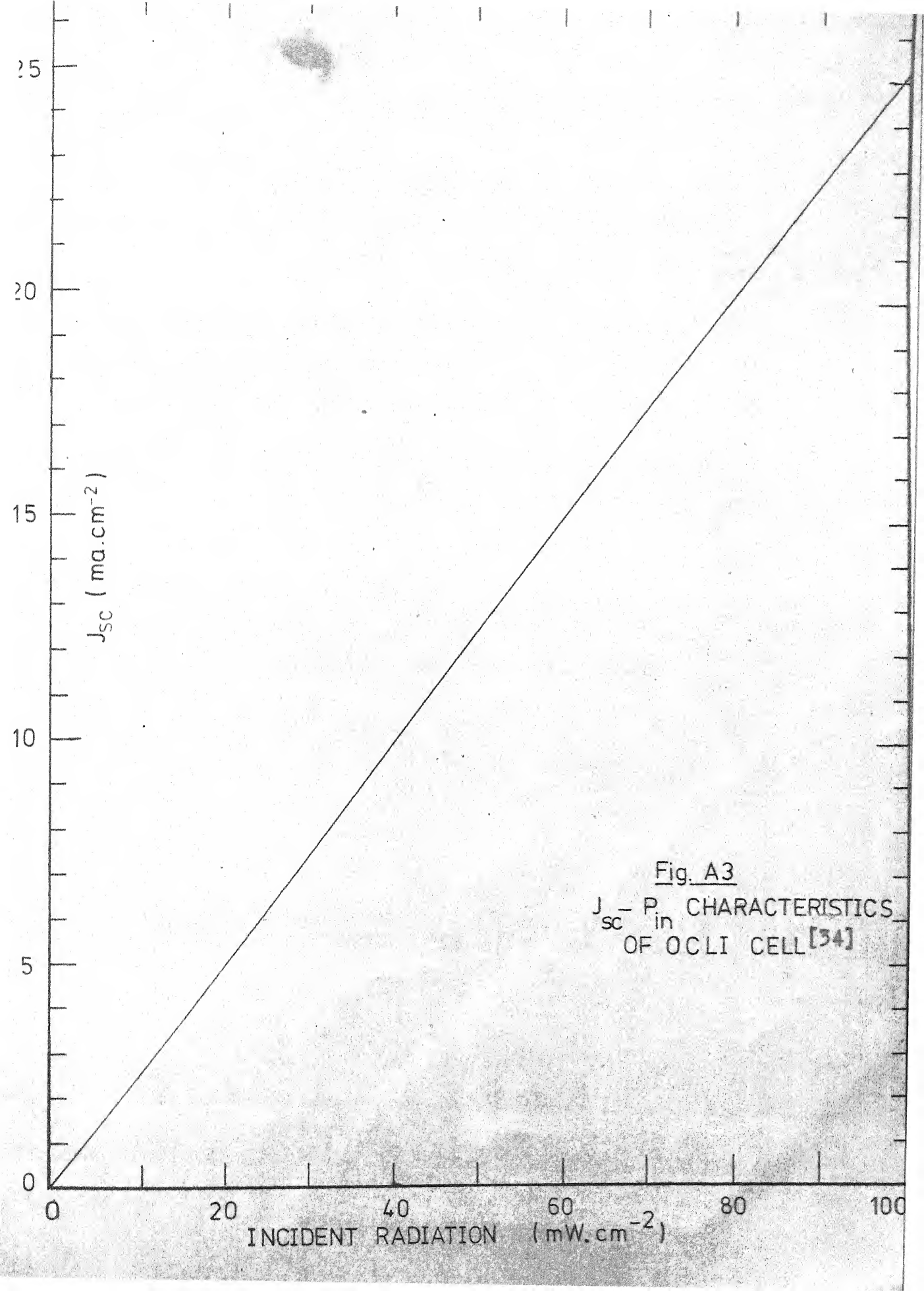

Fig. A3
$J_{sc} - P_{in}$ CHARACTERISTICS OF OCLI CELL [34]

The transmittance measurements made with the help of this solar cell and with photo electric colorimeter (ERMA AE11) are found to be in close agreement (deviation $< 4\%$).